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FINAL
Examination Paper

(COVER PAGE)

Session	:	**April 2016**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 2101: Introduction to Digital Electronics**
Date of Examination	:	29 July 2016, Friday
Time	:	8.00am – 10.00am Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Nil

Examiner(s) : **Mr. Steven Khoo Boo Tap**

Moderator : Mr. Kevin Tan

This paper consists of 11 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: APRIL 2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the number 0 through 9, respectively, as shown below in Figure 1(a-1). The BCD inputs are labelled as RSTU, R is the MSB and U is the LSB. Figure 1(a-2) shows a Common-Anode 7 segment display. Assume all unused inputs as don't care.

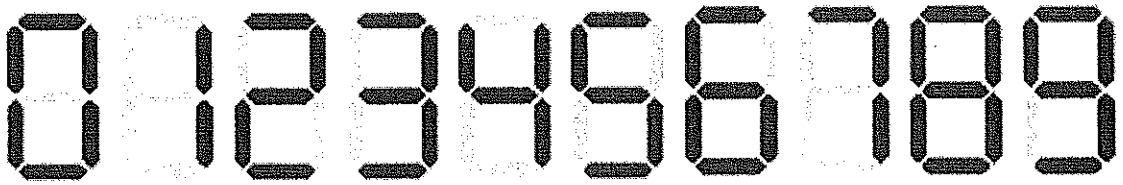


Figure 1(a-1)

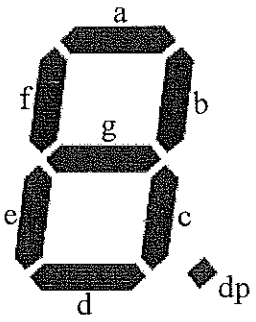


Figure 1(a-2)

(i) Develop the truth table for the inputs to segments a through g of the 7 segment.
(4 marks)

(ii) Determine the SOP form of the logic expression for segments e and f.
(6 marks)

(iii) Implement the logic expression using only 2-input NAND gate with minimum IC consideration. State the number of ICs used. Show all working clearly.
(7 marks)

(b) Using Boolean algebra only, simplify to the simplest SOP form:

(i) $F_1 = XY\overline{Z} + \overline{X\left(\overline{Y} + \overline{Z}\right)\left(Y + Z\right)}$

(4 marks)

(ii) $F_2 = \overline{X} \cdot \overline{Y} \cdot Z + X \cdot Y \cdot Z + \overline{X} \cdot \overline{Y} \cdot \overline{Z} + \overline{X} \cdot Y \cdot Z + X \cdot \overline{Y} \cdot Z$

(4 marks)

Question 2

(a) Design a synchronous 3-bit counter using positive edge-triggered JK flip-flops as shown in Figure 2(a) below. Assume all unused states as don't care. Use $Q_2Q_1Q_0$ outputs labelling for J_2K_2, J_1K_1 and J_0K_0 inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.

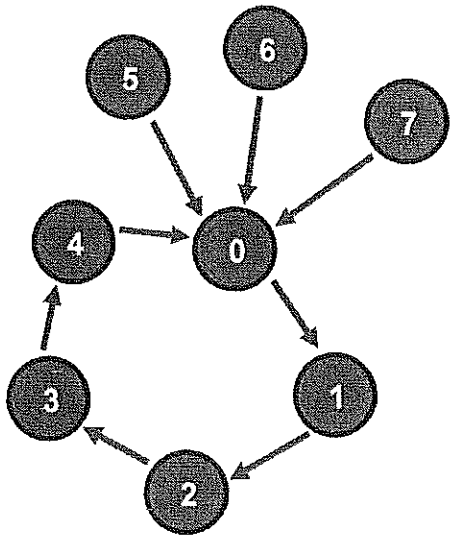


Figure 2(a)

(i) Provide the excitation table used.

(1 mark)

(ii) Provide the transition table/ next state table.

(4 marks)

(iii) Simplify using Karnaugh map and Boolean algebra if necessary.

(3 marks)

(iv) Draw the complete logic circuit diagram with proper label.

(4 marks)

(b) Design a synchronous 3-bit counter that counts in the sequence 101 ⇨ 010 ⇨ 000 ⇨ 111 ⇨ 101. Choose a suitable type of flip flops to use for this design such as D flip flops only or T flip flops only or JK flip flops only or RS flip flops only. Also, use an appropriate control signal together with flip flops of your choice to load the initial value 101 for the counter using a single reset signal. Assume all unused states as don't care. Use $Q_2Q_1Q_0$ as output labelling. Provide proper labelling for the designed logic circuit. Show all workings clearly.

(i) Provide the excitation table used.

(1 mark)

(ii) Provide the transition table/ next state table.

(4 marks)

(iii) Simplify using Karnaugh map and Boolean algebra if necessary.

(4 marks)

(iv) Draw the complete logic circuit diagram with minimum components consideration.

(4 marks)

Question 3

(a) Table 3(a) show a portion of a dual positive edge-triggered JK flip-flops (DM7476) datasheet. Figure 3(a) show the logic circuit diagram of an asynchronous counter which uses positive edge-triggered JK flip-flops with labelling of $Q_AQ_BQ_CQ_D$ where Q_D is MSB and Q_A is LSB. Assume the environment is at $T_A = 25°C$ with $V_{CC} = 5V$.

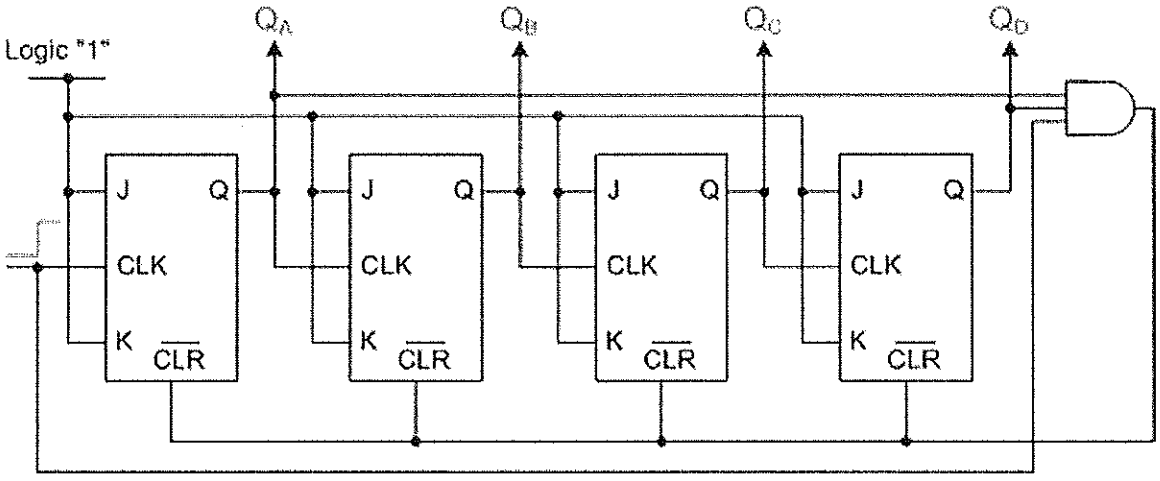


Figure 3(a)

Switching Characteristics
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25	ns

Table 3(a)

(i) Determine the total propagation delay from the given datasheet in Table 3(a). Assume the propagation delay for the 3-input AND gate is 30ns.

(5 marks)

(ii) Determine the maximum frequency at which the counter can be operated stably.

(3 marks)

(iii) Show the output timing diagram of Figure 3(a) and state the function of this counter.

(5 marks)

(b) Perform the following number system transformation. Show all workings clearly.

(i) $[3020.3020_8 - 1002.1002_8]$ to decimal equivalent with 9 decimal points accuracy.

(4 marks)

(ii) $[106.01_8 \times 1.6_8]$ to binary equivalent with 11 binary points accuracy.

(4 marks)

(iii) $[163.0703125_{10} - 11.101_8]$ to hexadecimal equivalent with 3 hexadecimal points accuracy.

(4 marks)

Question 4

(a) Assume that the numbering system used is a 10-bit system. Show all working clearly. Express the decimal number +128 and –128 in the sign-magnitude, 1's complement and 2's complement form as shown in the Table 4(a).

	+128	–128
Sign-magnitude		
1's complement		
2's complement		

Table 4(a)

(6 marks)

(b) Figure 4(b) below shows a 3-bit synchronous counter which is designed so that it performs a special counting sequence. Analyse its operation by determining its counting sequence. Switch S is a control signal used to control the sequence of the counting. Flip-flop FF2 is MSB and FF0 is LSB. Use $D_2T_1D_0$ inputs labelling for Q_2, Q_1 and Q_0 outputs. Show all workings clearly.

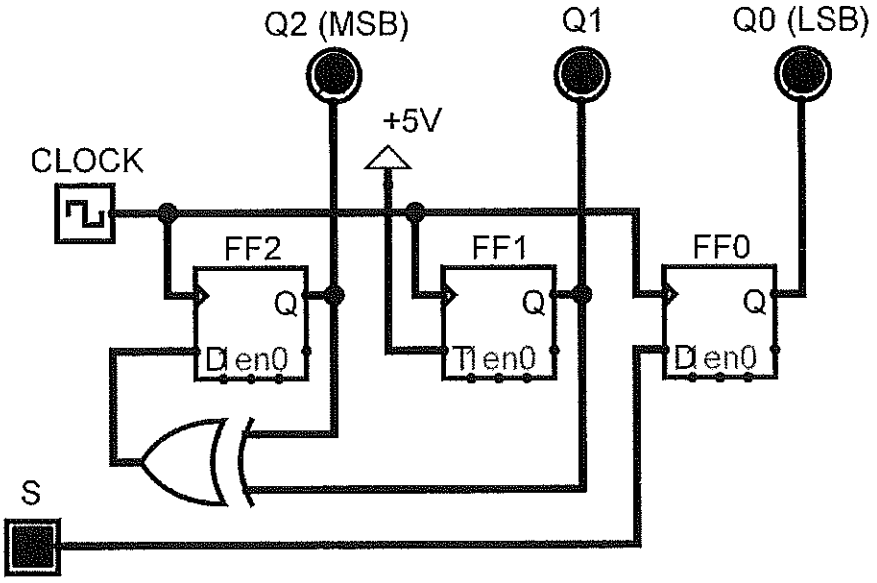


Figure 4(b)

(i) Provide the Boolean expressions from the logic circuit.

(1 mark)

(ii) Provide all Karnaugh maps according to the expressions.

(3 marks)

(iii) Provide the transition table/ next state table with excitation table.

(4 marks)

(iv) Draw the state diagram and comment on the outcome of the states obtained. What application can this circuit be used for?

(4 marks)

(c) A binary-weighted-input DAC is shown in Figure 4(c). If the LSB bit resistor has a value of 480kΩ, compute the values of the other input resistors. Also, calculate the V_{out} if the DAC has a binary input of 1010 with Logic 1 (HIGH) as +5.0V and Logic 0 (LOW) as 0V. Assume that R_f equals to 10kΩ. What are the disadvantages of this method of DAC?

(7 marks)

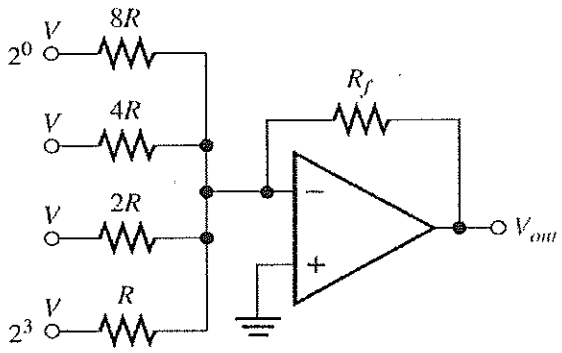
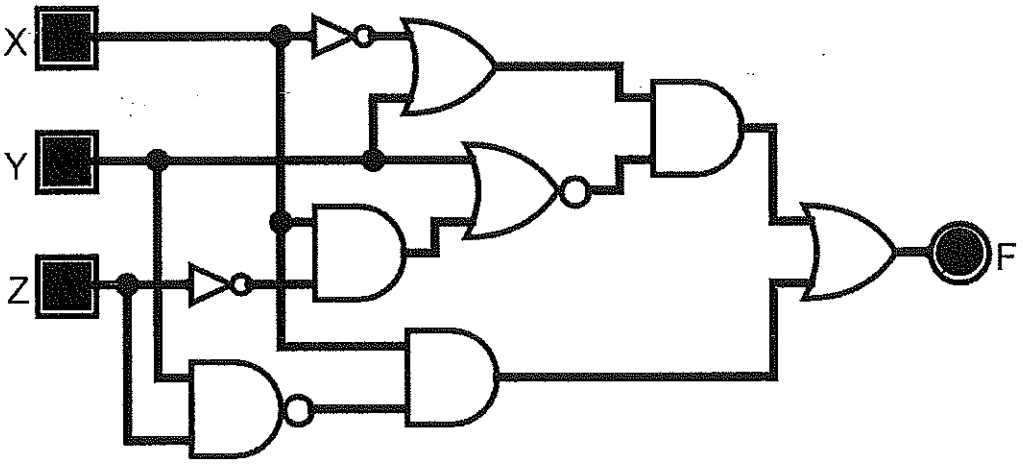


Figure 4(c)

Question 5

(a) Use the given Karnaugh map and/or Boolean algebra to obtain the minimum

(i) SOP expression for the logic circuit,



(5 marks)

(ii) POS expression for the truth table,

A	B	C	D	F
0	0	0	×	0
0	0	1	×	1
0	1	×	×	0
1	0	0	×	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	×	1

(3 marks)

(b) A circuit uses four switches to control four Motors as shown in Figure 5(b). The system uses four manual on/off switches, control logic, and motor drive interface to control the conveyor lubrication pump motor, the conveyor motor, the cross-cut saw motor, and band saw motor. Switch input S_1 controls the lubrication pump motor (output M_1). Switch input S_2 controls the conveyor motor (output M_2). Switch input S_3 control the band saw motor (output M_3). Switch input S_4 controls the cross-cut saw motor (output M_4) with those conditions as given by Table 5(b).

(i) Simplify the Boolean expression for motors, M_1 and M_3 using Karnaugh Map and/or Boolean Algebra to the simplest form.

(5 marks)

(ii) Design a minimized logic circuit using only 2-input NAND gate to control motors, M_1 and M_3. Compare the NAND gate design with 2-input NOR gate design. Also, state the number of IC used in each design.

(12 marks)

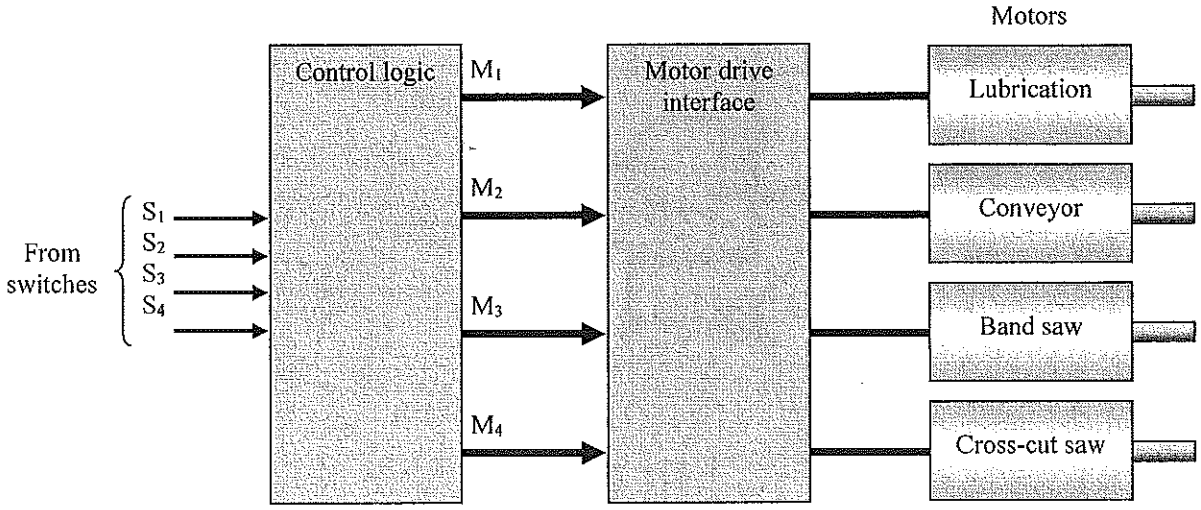


Figure 5(b)

Input Switches				Output Motors			
S_1	S_2	S_3	S_4	Lubrication (M_1)	Conveyor (M_2)	Band Saw (M_3)	Cross-cut Saw (M_4)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	0
0	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0
1	0	1	1	0	0	0	0
1	1	0	0	1	1	0	0
1	1	0	1	0	0	0	0
1	1	1	0	1	1	1	0
1	1	1	1	0	0	0	0

Table 5(b)

Question 6

(a) Figure 6(a) has three inputs (A, B, C) and two outputs (Y, Z).
Table 6a(i) shows a portion of quadruple 2-input AND gates datasheet.
Table 6a(ii) shows a portion of quadruple 2-input OR gates datasheet.
Table 6a(iii) shows a portion of quadruple 2-input XOR gates datasheet.

(i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly.

(6 marks)

(ii) What is minimum operating frequency that can be applied to this circuit without affecting the functionality of the circuit? State the function of this circuit.

(4 marks)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table 6a(i) AND gate

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 6a(ii) OR gate

Symbol	Parameter	Conditions	CL = 15 pF, RL = 400Ω		Units
			Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other input LOW		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other input HIGH		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table 6a(iii) XOR gate

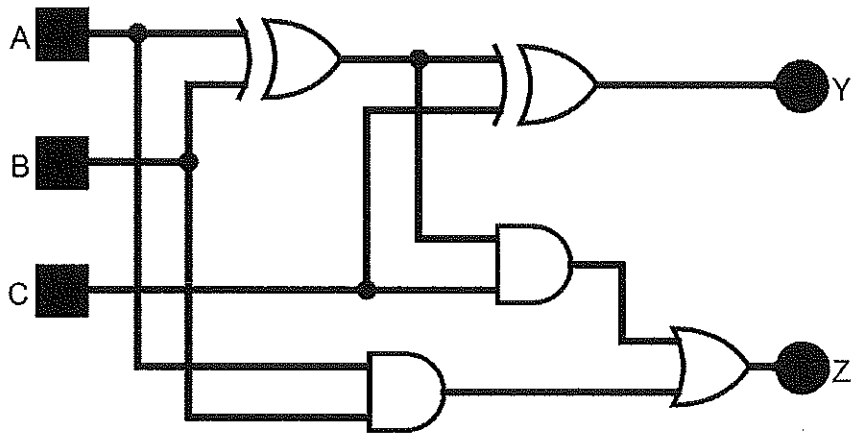


Figure 6(a)

(b) A 14-bit DAC produces an output current in proportion to its digital input. For a digital input of 00000001010000, an output current of 25mA is produced.

(i) What will the output current be if the digital input is 10010001111010?

(3 marks)

(ii) What is the maximum output current produced by this DAC?

(2 marks)

(iii) What should the digital input be if a 1205mA output current is required?

(2 marks)

(c) Table 6(c) shows the current ratings of TTL series logic gates. A 74S04 NOT gate output is driving 4 (FOUR) Standard TTL gate inputs, 7 (SEVEN) Advanced Low-Power Schottky TTL gate inputs, 6 (SIX) Fast TTL gate inputs and 5 (FIVE) Low-Power Schottky TTL gate input as shown in Figure 6(c). Determine if there is a loading problem.

(8 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

Table 6(c)

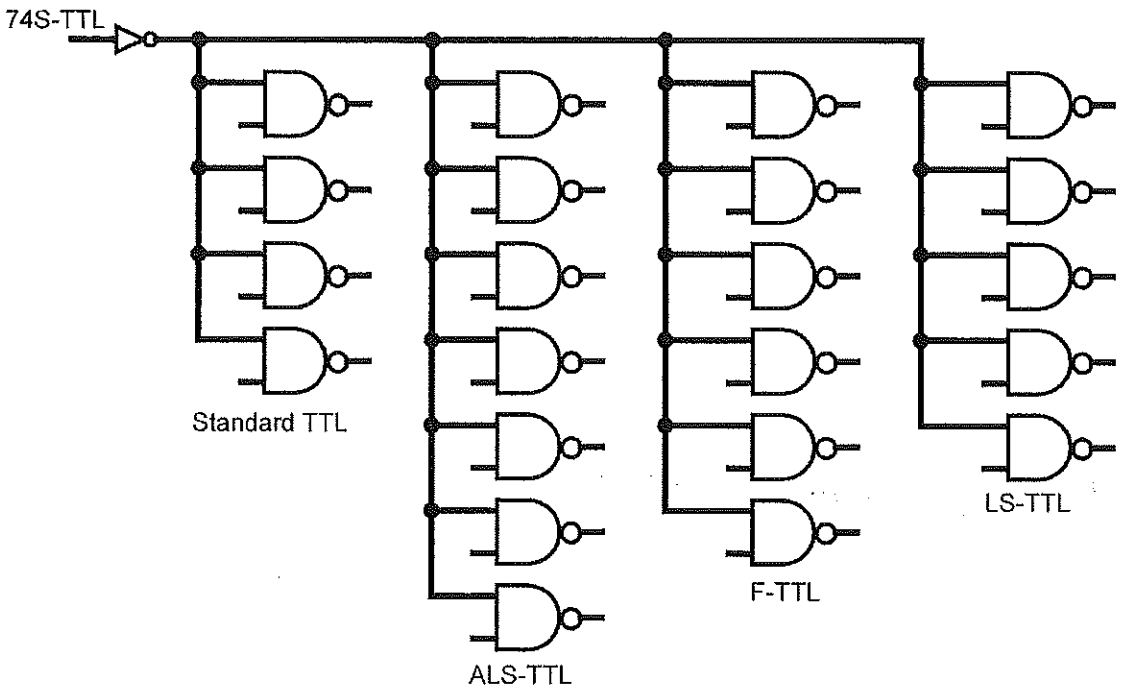


Figure 6(c)

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