INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	**April 2016**
Programmes	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE1106: Analogue Electronics**
Date of Examination	:	29 July 2016, Friday
Time	:	5.00pm – 7.00pm
Duration	:	2 Hours Reading Time : Nil
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.

Materials Permitted :
Scientific Calculator (Model fx570 Series)

Materials Provided :
Nil

Examiner(s)	:	**Mr. Chan Tse Wei**
Moderator	:	Dr. Khoo Bee Ee

*This paper consists of **8** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1106: ANALOGUE ELECTRONICS
FINAL EXAMINATIONS: APRIL 2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

a. Figure-Q1(a) shows the frequency response plot of a BJT-based, capacitor-coupled voltage amplifier. The amplifier voltage is terminated by a pure resistive load and is powered by a single DC voltage source.

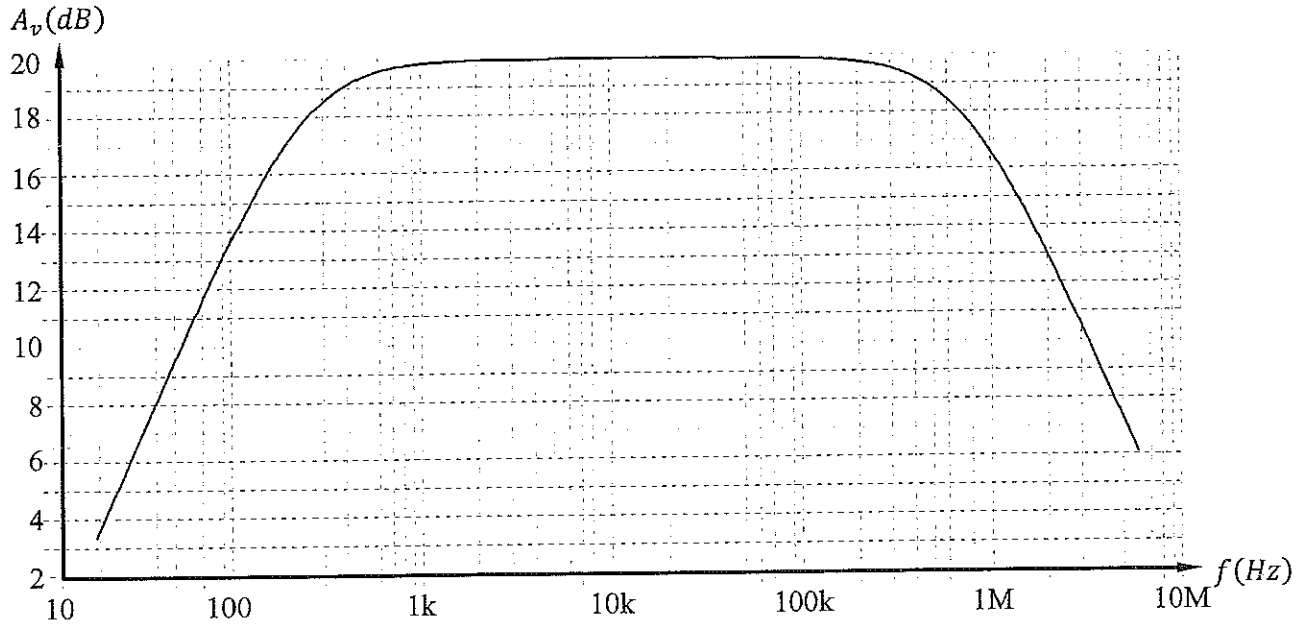

Figure-Q1(a)

i. Determine the maximum voltage gain of the amplifier in ratio. [3]

ii. Estimate from the frequency response plot, the bandwidth of the voltage amplifier. [6]

iii. Explain the root causes of the gain reduction at both ends of the frequency spectrum. [4]

iv. Estimate the gain reduction rate at the low frequency spectrum. [3]

b. Figure-Q1(b) shows the voltage amplifier circuit model that produces the frequency response plot shown in Figure-Q1(a). The amplifier has negligible output resistance.

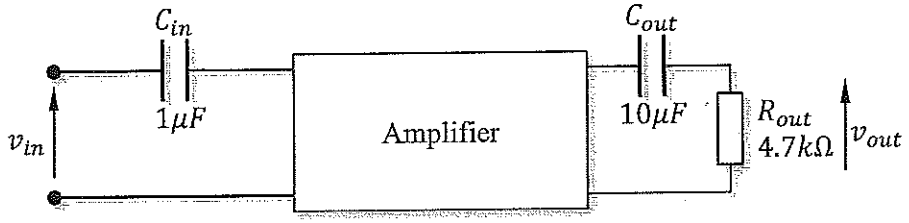

Figure-Q1(b)

i. Determine the input resistance of the voltage amplifier. [5]

ii. Determine the peak current amplitude that flows through R_{load} if v_{in} is a 1 V peak voltage at 10 kHz. [4]

Question 2

a. What is the quantitative difference between a small signal BJT and a power BJT in terms of,

i. collector current capacity? [3]

ii. current gain capacity? [3]

b. i. State the common approach taken to operate a power transistor under its safe operating area, other than by controlling its electrical quantities. [3]

ii. How do class D power amplifiers differ from class A, B and C power amplifiers in terms of their transistor biasing? [3]

iii. The conduction cycle of the transistor in a class B power amplifier is only 180°. How does the power amplifier produce a replica of its input signal if the input signal oscillates for 360°? [3]

c. Suggest the most appropriate power amplifier (either class A, B, or C) for each of the following application requirements:

i. Stays cool in the absence of input signal and when input signal is applied, minor output distortion is tolerable. [2]

ii. 1 W to 2 W output stage headphone amplifier. [2]

iii. Amplifier is to deal with radio frequency signal, needs to be highly efficient, up to 80%. [2]

d. 15W of DC power is drawn by a power amplifier. If 3W of the power is dissipated as heat by the power transistor and its biasing component, how much power is delivered to the load? What is the efficiency of the power amplifier? [4]

Question 3

a. i. Explain the reason for the open-loop voltage gain of an op-amp being designed with a value much higher than the value commonly required by most electronic circuits? [3]

ii. State two advantages that a JFET-base op-amp has over a BJT-based op-amp. [4]

b. The op-amp in the circuit of Figure-Q3(b) is assumed ideal.

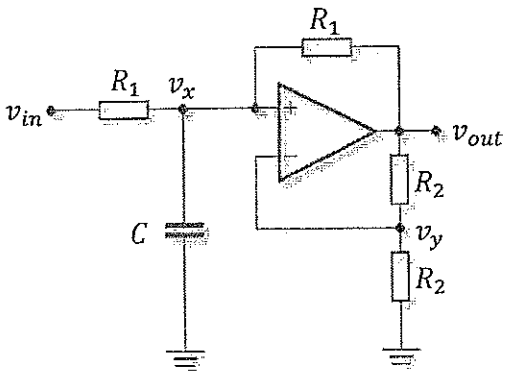

Figure-Q3(b)

i. Comment on the relationship between the node voltages v_x and v_y. [2]

ii. Write the nodal equation at node-v_y in its Laplace transformed domain. [2]

iii. Write the nodal equation at node-v_x in its Laplace transformed domain. [3]

iv. Making use of the nodal equations obtained in part (b)(i) and (iii), derive the instantaneous expression of the output voltage, $v_{out}(t)$ in terms of $v_{in}(t)$, R_1 and C. [5]

v. Hence, determine the function of the circuit base on the output expression obtained in part (b)(iv). [3]

vi. Briefly describe the output waveform, if a square wave is applied to the circuit. Assume that the op-amp does not saturate. [3]

Question 4

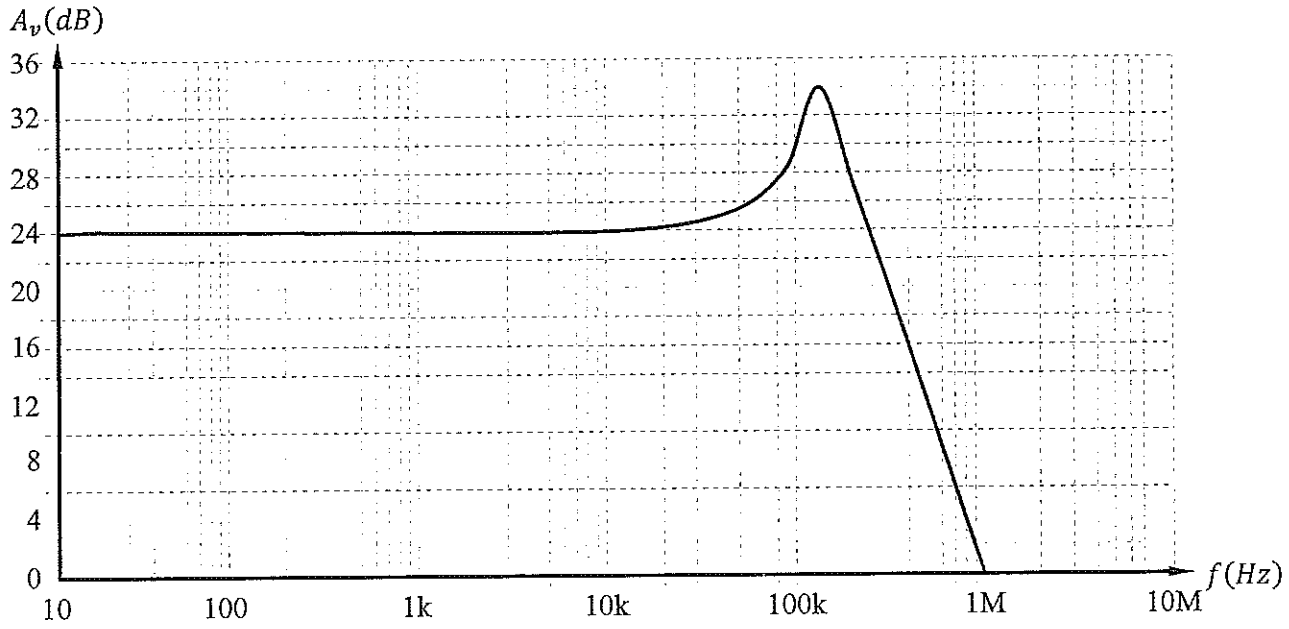

Figure-Q4(a)

a. Figure-Q4(a) shows the frequency response of a filter circuit.

i. Which type of filter circuit does this frequency response belongs to? [1]

ii. Predict the DC gain value of the filter circuit. [1]

iii. State the order of the filter circuit. Justify your answer. [4]

iv. "This filter exhibits Butterworth filter characteristic." Is this statement correct? Justify your answer. [4]

v. What is the frequency range where attenuation actually took place? Justify your answer. [4]

b. Design a passive twin-T notch filter to filter the 50 Hz mains hum signal. Show all design steps clearly. Determine the bandwidth of the notch filter. [11]

Question 5

a. State if each of the following statements is "True" or "False".

i. An electronic oscillator is a circuit that generates an output that swings between two distinctive levels periodically. [1]

ii. All oscillator circuits produce output signals that replicate a sinusoidal wave. [1]

iii. A harmonics oscillator can be used to generate radio wave called as carrier signal. [1]

iv. Timer circuit utilizes oscillator to keep track of time. [1]

v. All microprocessors must have oscillator circuits to support their operation. [1]

vi. The 555 timer can be used to generate a rectangular wave up to 10 MHz. [1]

vii. A low pass filter can be used to produce a sinusoidal wave by connecting it to a square wave oscillator. [1]

viii. Oscillators built on the basis of crystal or tunnel diode are classified as negative resistance oscillators. [1]

ix. Colpitts, Hartley and Clapp oscillators are examples of feedback oscillators. [1]

x. To ensure proper operation of a relaxation oscillator, the Barkhausen criteria of oscillation must be fulfilled. [1]

b. Figure-Q5(b) shows an improved version of the phase shift oscillator.

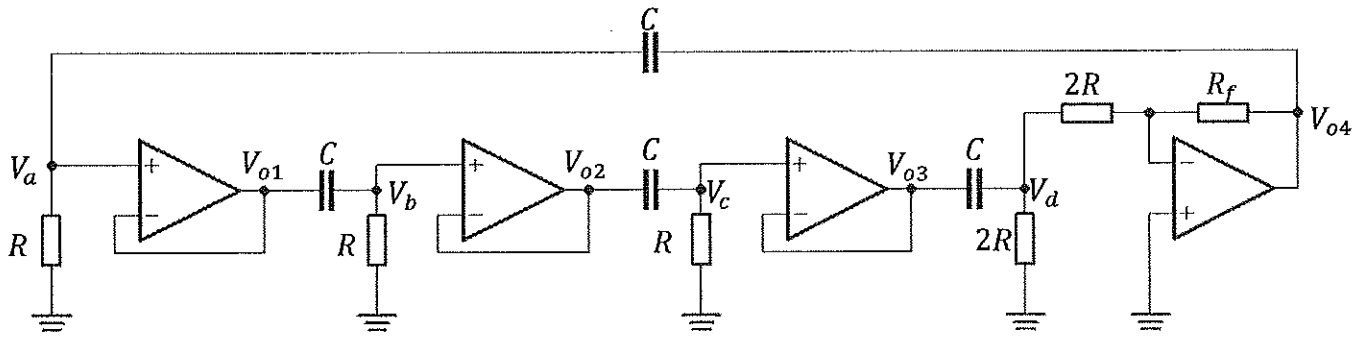

Figure-Q5(b)

i. State the phase shift between V_d and V_{o4}. [2]

ii. To sustain oscillation, state the required phase shift between V_{o4} and V_a. [3]

iii. Explain the purpose of the three buffer circuits in the oscillator. [2]

iv. Derive the relationship of R and C and the frequency of oscillation. [4]

v. Derive the amplifier gain value of the oscillator if oscillation is sustained. [4]

Question 6

a. Figure-Q6(a) shows an incomplete block diagram of an audio amplifier system. Complete the block diagram by copying it into your answer booklet and label all the blank blocks. [6]

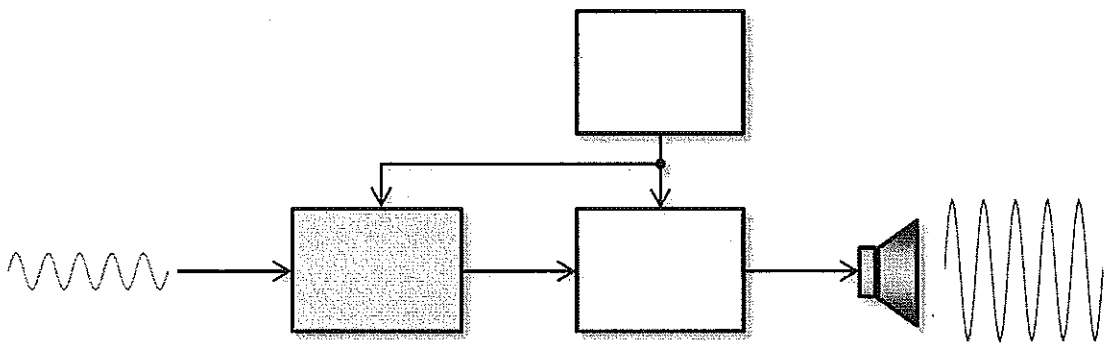

Figure-Q6(a)

b. Figure-Q6(b) shows the high frequency AC model of a common source amplifier circuit. The mid-band voltage gain $v_{out}/v_{gs} = -80$.

Show that its upper cutoff frequency is approximately 727 kHz. [12]

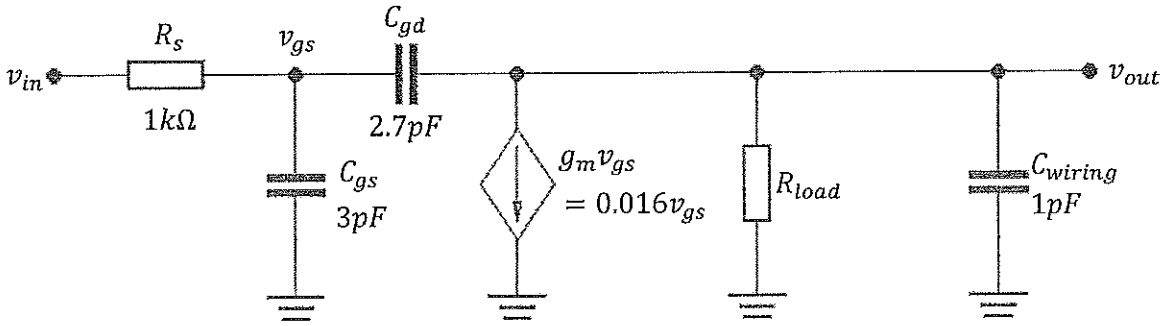

Figure-Q6(b)

c. Design a single op-amp circuit to implement the following expression:

$$v_{out} = \frac{v_1 + v_2 + v_3}{3}$$

Show all design steps clearly. [7]

~ The End ~