INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	**April 2016**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 1105: Circuit Theory & Electronic Devices**
Date of Examination	:	2 August 2016, Tuesday
Time	:	8.00am – 10.00am
Duration	:	2 Hours Reading Time : Nil
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : **THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL**

Materials Permitted :
Non-Programmable Scientific Calculator

Materials Provided :
Answer Booklet

Examiner(s)	:	**Ms. Shalyn Lim Sheue Hui**
Moderator	:	Mr. Kevin Tan

This paper consists of 13 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEI)
EEE 1105: CIRCUIT THEORY & ELECTRONIC DEVICES
FINAL EXAMINATION: APRIL 2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) With reference to Figure Q1(a) , calculate

(i) the total resistance. (3 marks)

(ii) the current, I. (2 marks)

(iii) the currents, I_8. (4 marks)

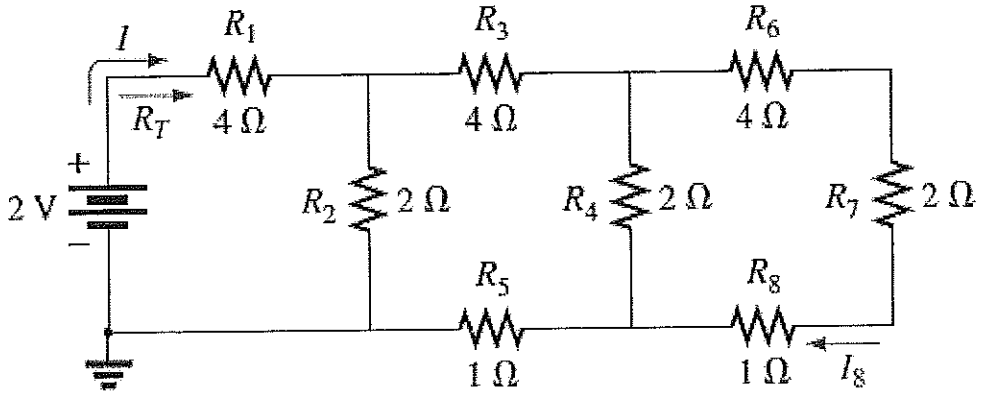

Figure Q1(a)

(b) Given the voltmeter reading V =27 V in Figure Q1 (b) (i). Is the network operating properly? not, what could be the cause of the incorrect reading?

(4 marks)

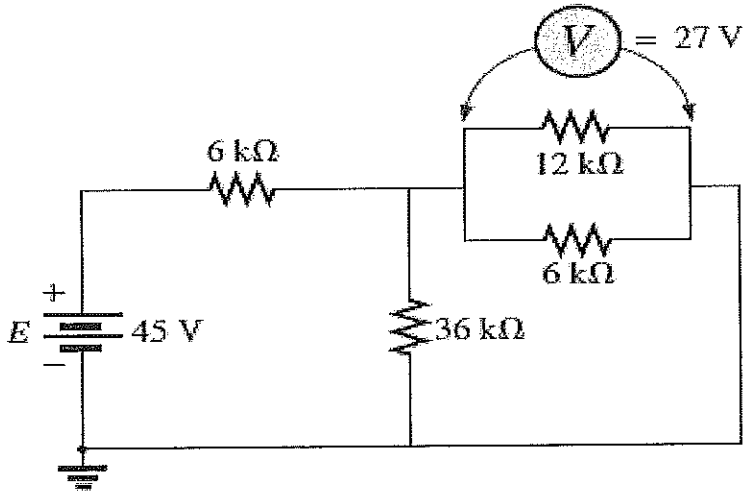

Figure Q1(b)

(c) With reference to Figure Q1(c). Calculate voltage drop across 4Ω resistor using ***Nodal Analysis***.

(5 marks)

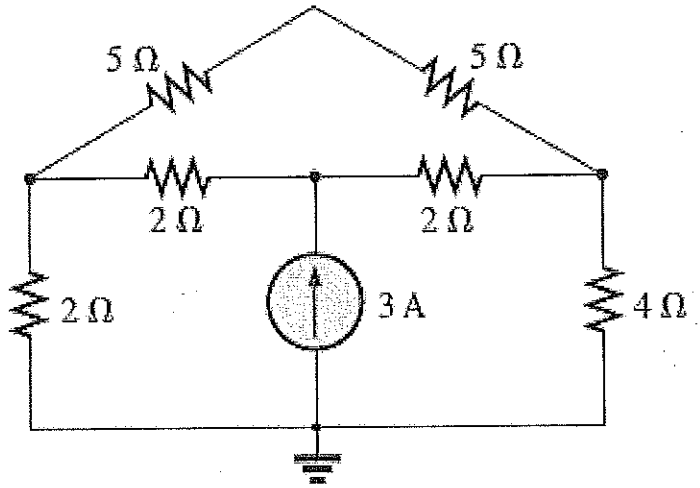

Figure Q1(c)

(d) Calculate the maximum power transfer to R for the network shown in Figure Q1(d)

(7 marks)

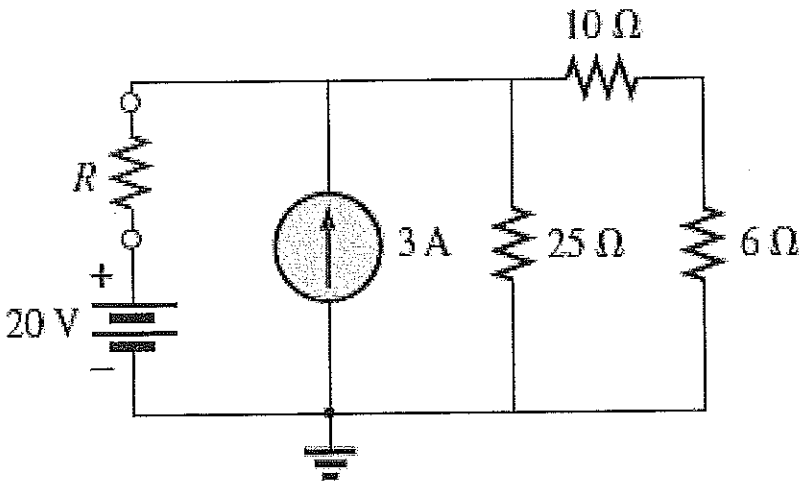

Figure Q1(d)

Question 2

(a) For the following pairs of voltages and currents, indicate whether the element involved is a capacitor, an inductor, or a resistor, and the value of C, L or R if sufficient data are given

$$v = 550\sin(377t + 50°)$$
$$i = 11\sin(377t - 40°)$$

(3 marks)

(b) An electrical system is rated 10 kVA, 200 V at a 0.5 leading power factor.

(i) Determine the impedance of the system in complex form.

(3 marks)

(ii) Find the average power delivered to the system.

(2 marks)

(c) For the network of Figure Q2(c),given the rms of the supply voltage is $100\ \angle 0°$ V determine
[Note: answer in polar form]

(i) the total admittance Y_T.

(4 marks)

(ii) the voltage V_1 and V_2 .

(4 marks)

(iii) the current I_3.

(3 marks)

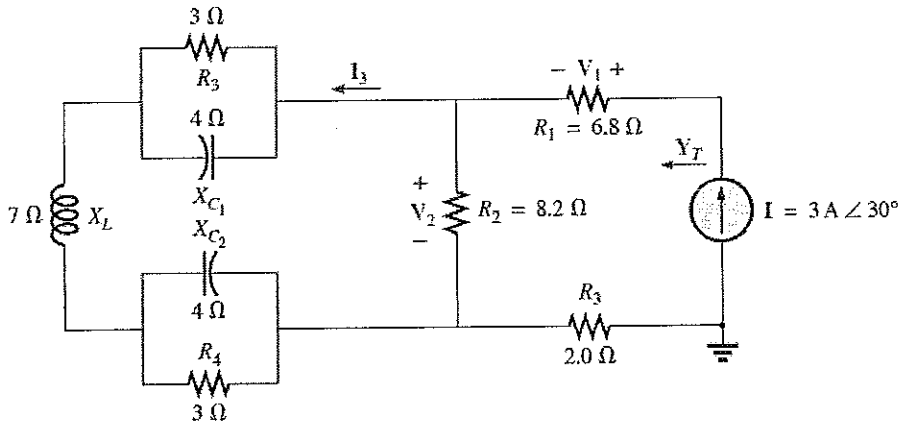

Figure Q2(c)

(d) Find the element or elements that must be in the closed container in Figure Q2(d) to satisfy the following conditions in (I) and (II).

(I) Average power to the circuit =3000 W.
(II) Circuit has a lagging power factor.

(6 marks)

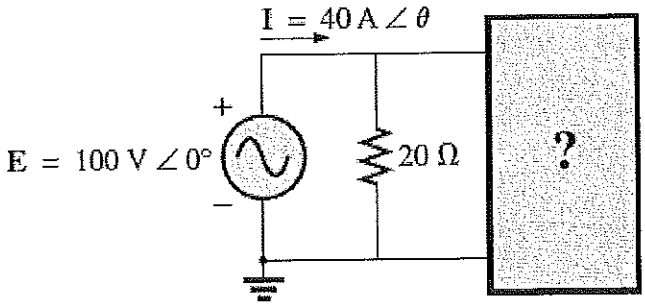

Figure Q2(d).

Question 3

(a) By using a diagram with the **detail label** of electric field and charges, explain the process of forming the depletion region in P-N junction.

(5 marks)

(b) The circuit as shown in Figure Q3 (b) contains two silicon diodes D1 and D2. Calculate the values of their respective currents, I_1, I_2 and I_3.

(5 marks)

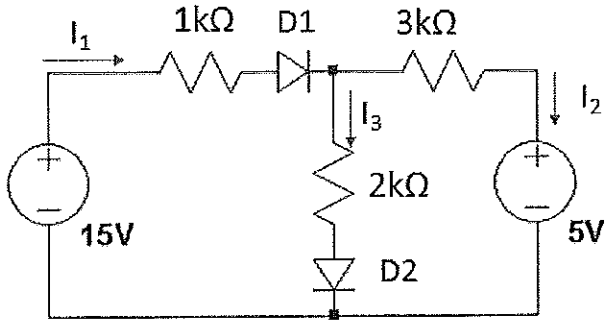

Figure Q3(b)

(c) Figure Q3 (c) shows the full wave rectifier circuit with the input sine wave.

(i) Calculate the average output voltage, V_{AVG}.

(4 marks)

(ii) Determine the value of PIV.

(2 marks)

(iii) Sketch the output voltage at RL with proper labeling.

(2 marks)

(iv) Calculate the average diode current.

(3 marks)

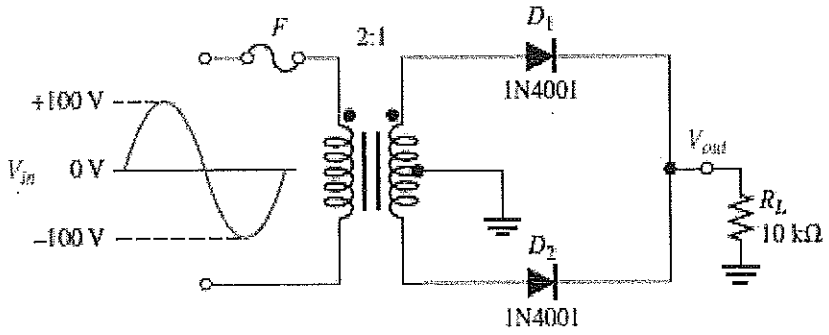

Figure Q3(c)

(d) Sketch Vo for the network of Figure Q3(d) and determine the average output current. (5 marks)

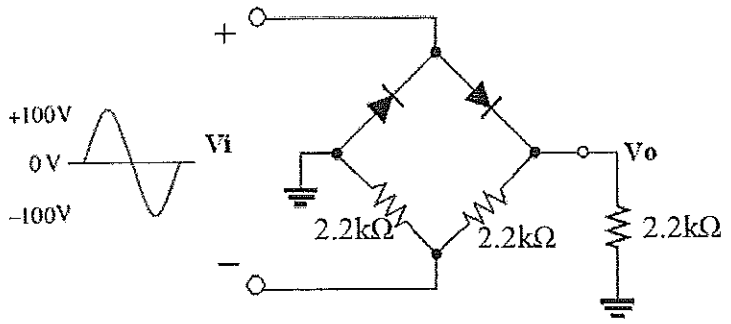

Figure Q3(d)

Question 4

(a) Using the load line analysis sketch and label the operating regions of the BJT. Why the setting of Q-point (dc operating point) is important?

(7 marks)

(b) Determine I_B,I_C and V_{CE} for the network shown in Figure 4(b) with β=50

(5 marks)

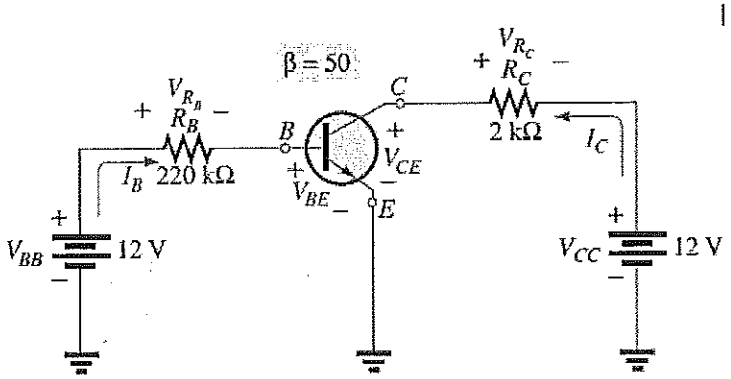

Figure 4(b)

(c) Given the emitter-bias configuration network of Figure Q4(c) with the given V_B and V_{BE} and the approximation $I_C \approx I_E$ is often applied to transistor networks.

(i) Determine V_E and I_E.

(4 marks)

(ii) Calculate V_1.

(3 marks)

(iii) Determine V_{BC}.

(4 marks)

(iv) Calculate V_{CE}.

(2 marks)

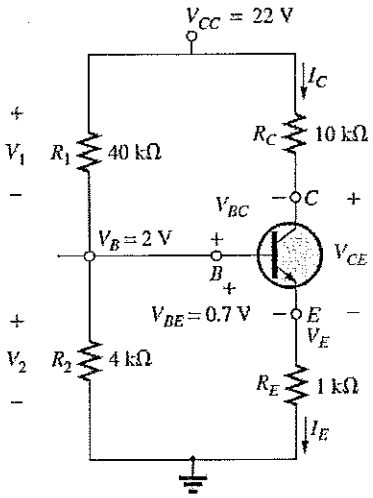

Figure Q4(c)

Question 5

(a) What are the advantages and disadvantages of FET compare to BJT.

(4 marks)

(b) The specifications of the n-channel E-MOSFET are given as: $V_{GS(Th)} = 4$ V and $I_{D(on)} = 4$ mA at $V_{GS(on)} = 6$ V, determine k and write the general expression for the drain current, I_D. Sketch the transfer characteristics for this device.

(6 marks)

(c) For the FET as shown in Figure Q5(c) , calculate

(i) the voltages V_G and V_S.

(4 marks)

(ii) the currents I_1, I_2, I_D and I_S.

(6 marks)

(iii) the V_{DS} and V_{DG}

(5 marks)

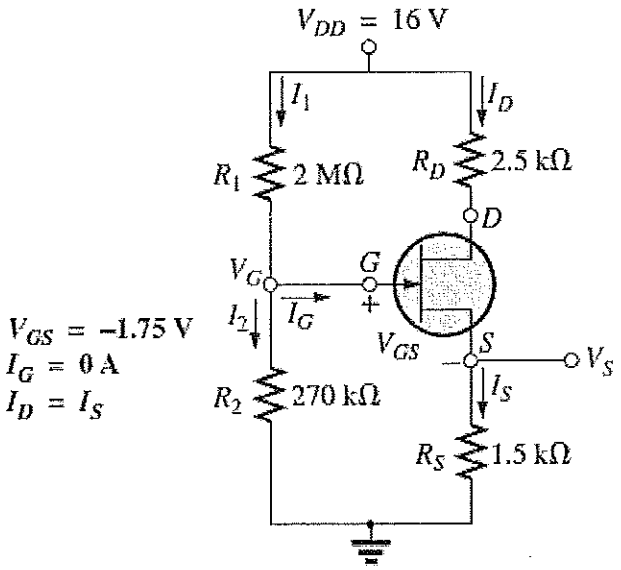

Figure Q5(c)

Question 6

(a) Refer to the circuit shown in Figure Q6 (a), find

(i) the currents I_2, I_6, and I_8.

(7 marks)

(ii) the voltages V_4 and V_8.

(4 marks)

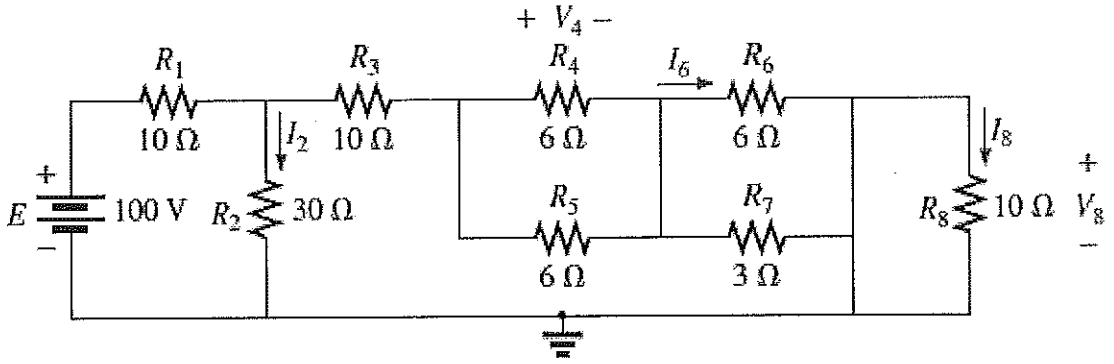

Figure Q6(a)

(b) Find the Norton equivalent circuit for the shaded area of the network to the left of a-b in Figure Q6(b).

(6 marks)

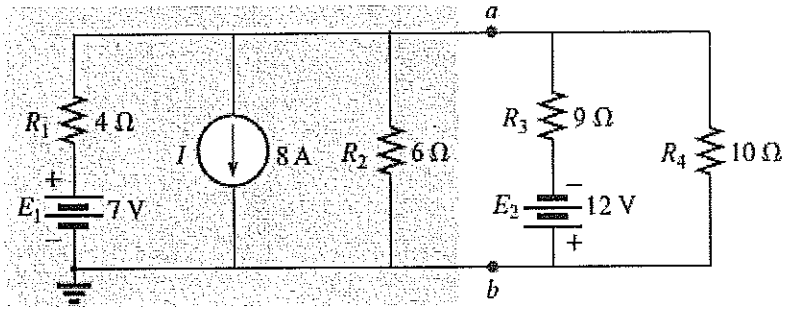

Figure Q6(b)

(c) The biasing circuit of Figure Q6 (c) has current gain $\beta = 200$. Assume $V_{BE} = 0.7$ V.

(i) Calculate the quiescent operating point.

(5 marks)

(ii) Sketch the load line, properly labeling the saturation and cut-off points

(3 marks)

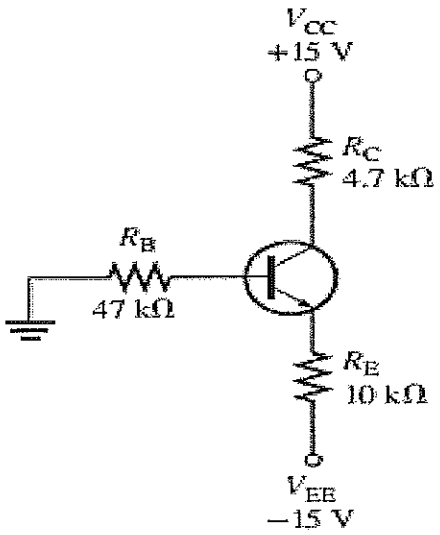

Figure Q6(c)

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EEE1105(F)APRIL16Shalyn Lim 28/06/16