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FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2017**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 2114: Introduction to Embedded Systems**
Date of Examination	:	14 December 2017 (Thursday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Appendix A, Appendix B, Appendix C & Appendix D

Examiner(s) : **Mr. Steven Khoo Boo Tap**

Moderator : Mr. Kevin Tan Geok Su

*This paper consists of **13** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2114: INTRODUCTION TO EMBEDDED SYSTEMS
FINAL EXAMINATION: AUG2017 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Name and describe the function of the following labels in Figure 1(a) as shown below.

(i) Label (A) (3 marks)

(ii) Label (B) (3 marks)

(iii) Label (C) (3 marks)

State the possible type of microcontroller for Figure 1(a) internal architecture. (1 mark)

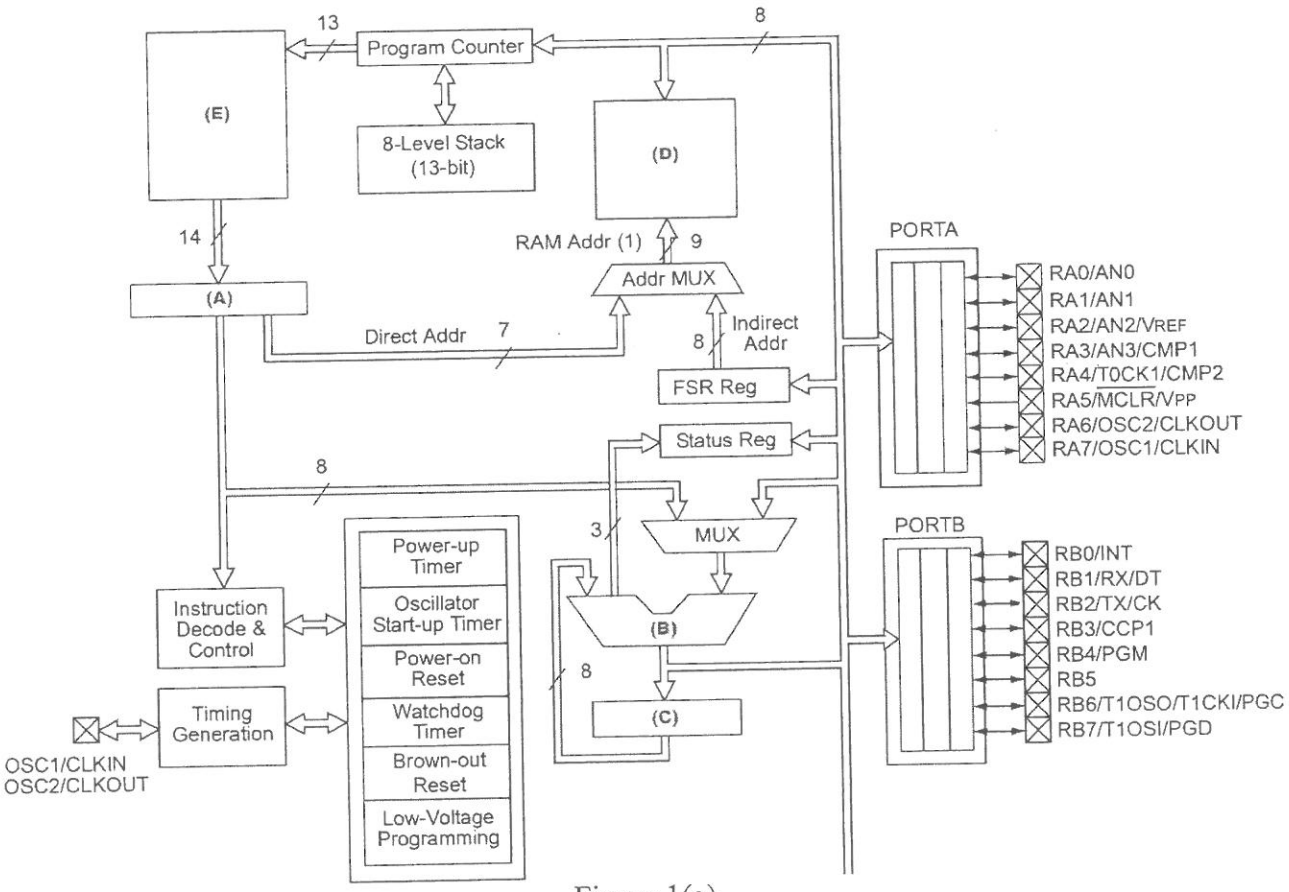

Figure 1(a)

(b) Table 1(b) assembly program will be built using MPLAB IDE with MPASMWIN assembler. Study and analyze the Assembly Language Codes given below written using PIC16F628A microcontroller and answer the following questions.

Table 1(b) PIC16F628A Assembly Coding

```
Line 1   INCLUDE <PIC16F628A.inc>
Line 2   __CONFIG 3F38H
Line 3   STATUS EQU 0x3
Line 4   ORG 0
Line 5          movf    22H,W
Line 6          addwf   32,0
Line 7          btfss   STATUS,C
Line 8          goto    NC
Line 9          clf     0x41,1
Line 10         incf    41H,F
Line 11         movwf   .66
Line 12         movf    h'21',0
Line 13         addwf   b'110001',W
Line 14         addwf   41h,1
Line 15         goto    A
Line 16  NC     movwf   o'102'
Line 17         movf    21H,0
Line 18         addwf   0x31,W
Line 19         movwf   d'065'
Line 20  A      goto    A
Line 21  END
```

(i) Identify significant **ERROR(S)** in the instructions of Table 1(b) that will caused the assembler to output "BUILD FAILED" when build all. Explain why it is incorrect and write the correct codes according to the Assembly Language format. Indicate the Line number of the error code as well.

(3 marks)

(ii) Based on the assumption that all lines of codes are corrected, what is the function of the program and also provide final result of Table 1(b) program after correction?

(4 marks)

(iii) Reduce the number of lines for the program in Table 1(b) as much as possible but still perform the same outcome as the original function of the coding? Hint: The improved full program should be less than 15 lines of coding instead of 21 lines.

(8 marks)

Question 2

(a) Given the Special Function Registers and File Registers as follows:

Table 2(a)(i) Special Function Registers

Update	Address	Symbol Name	Value
		WREG	32
	003	STATUS	00011001
	004	FSR	176
	006	PORTB	0X00
	086	TRISB	11111111

Table 2(a)(ii) File Registers

Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
000	--	00	00	19	B0	00	00	--	--	--	16	77	00	--	00	00
010	10	20	00	--	--	00	55	33	60	00	00	--	--	--	--	00
020	61	12	10	56	34	18	52	AA	11	33	22	44	50	60	78	80
030	14	24	34	45	54	64	74	84	94	A4	B4	C4	D4	E4	F4	04
040	21	31	41	51	62	71	81	91	01	02	03	04	05	06	07	08
050	09	0A	0B	0C	0D	E0	0E	0F	F0	35	36	37	38	39	40	42
060	42	46	47	48	49	56	85	57	58	59	5A	5B	5C	5D	5E	5F
070	63	65	66	67	68	69	6A	6B	6C	6D	6E	6F	72	73	74	75
080	--	FF	00	19	B0	FF	FF	--	--	--	16	77	70	--	08	--
090	--	--	FF	--	--	--	--	--	02	79	7A	7B	0C	00	--	6E
0A0	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	92	93
0B0	94	95	96	97	98	99	9A	9B	9C	9D	9F	9E	A0	B0	C0	D0
0C0	E0	F0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE
0D0	10	0A	44	12	23	34	45	56	67	78	89	9A	AB	BC	CD	DE
0E0	20	1C	EF	F0	01	23	45	67	89	AB	CD	EF	01	02	03	04
0F0	30	05	06	07	35	08	09	0A	0B	0C	0D	0E	0F	19	90	70

(All data of File Register are hexadecimal)

Perform the following short programs. Indicate the result of the affected register(s) and Status (Z, DC and C). The questions are independent of each other. Show all workings of **before** and **after** the execution of each instruction with appropriate diagram/table illustration of the affected register(s).

(i)
```
RLF     FSR,1
ANDWF   INDF,F
SWAPF   0x21,F
```
(5 marks)

(ii)
```
COMF    FSR,F
ADDWF   INDF,0
IORWF   b'1110110',1
```
(5 marks)

(iii)
```
MOVF    O'140',W
SUBWF   INDF,W
XORWF   FSR,1
```
(5 marks)

(b) Design a 4-bit binary counter using PIC16F628A microcontroller. The 4-bit (RB0-RB3) output pin should be connected to four LEDs via 330Ω resistors for each pin. Assume that the 1-second subroutine delay program is available. Write a program that will produce a binary sequence counting from 0000 to 1111 and repeat. Also, provide the complete circuit and include comments for all instructions used.

(10 marks)

Question 3

(a) Figure 3(a) below shows the Port B Functions of PIC16F877A microcontroller. Pin RB4:RB7 of PIC16F877A are normally used in keypad interfacing, explain why? Sketch the circuit diagram connection of Port B of PIC16F877A microcontroller and the 4 × 4 matrix keypad.

(7 marks)

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit 1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit 2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM(3)	bit 3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit 4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit 5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit 6	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit 7	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode or in-circuit debugger.

3: Low-Voltage ICSP Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

Figure 3(a)

(b) Provide THREE (3) major differences between PIC16F628A microcontroller and PIC16F877A microcontroller in term of technical aspect such as the internal architecture. Assuming cost and pin count of the microcontroller are not the main differences.

(6 marks)

(c) What is the main difference between an assembler directive and an assembly instruction?

(4 marks)

(d) The block diagram of the PIC16F877A analogue to digital converter (ADC) is shown in Figure 3(d)(i). The ADCON0 and ADCON1 registers are shown in Figure 3(d)(ii) and Figure 3(d)(iii) respectively. In this design, an internal voltage reference is selected, input channel 3 is selected, and the ADC is switched on but not running. Assume that channel 0, channel 1, channel 2 and channel 4 are configured as analogue input only. Also, assume that the conversion clock used is Fosc/4 with left justification on the result.

(i) What is the setting of the ADCON0 register?

(2 marks)

(ii) What is the setting of the ADCON1 register?

(2 marks)

(iii) Give one advantage of using an internal voltage reference or an external voltage reference.

(4 marks)

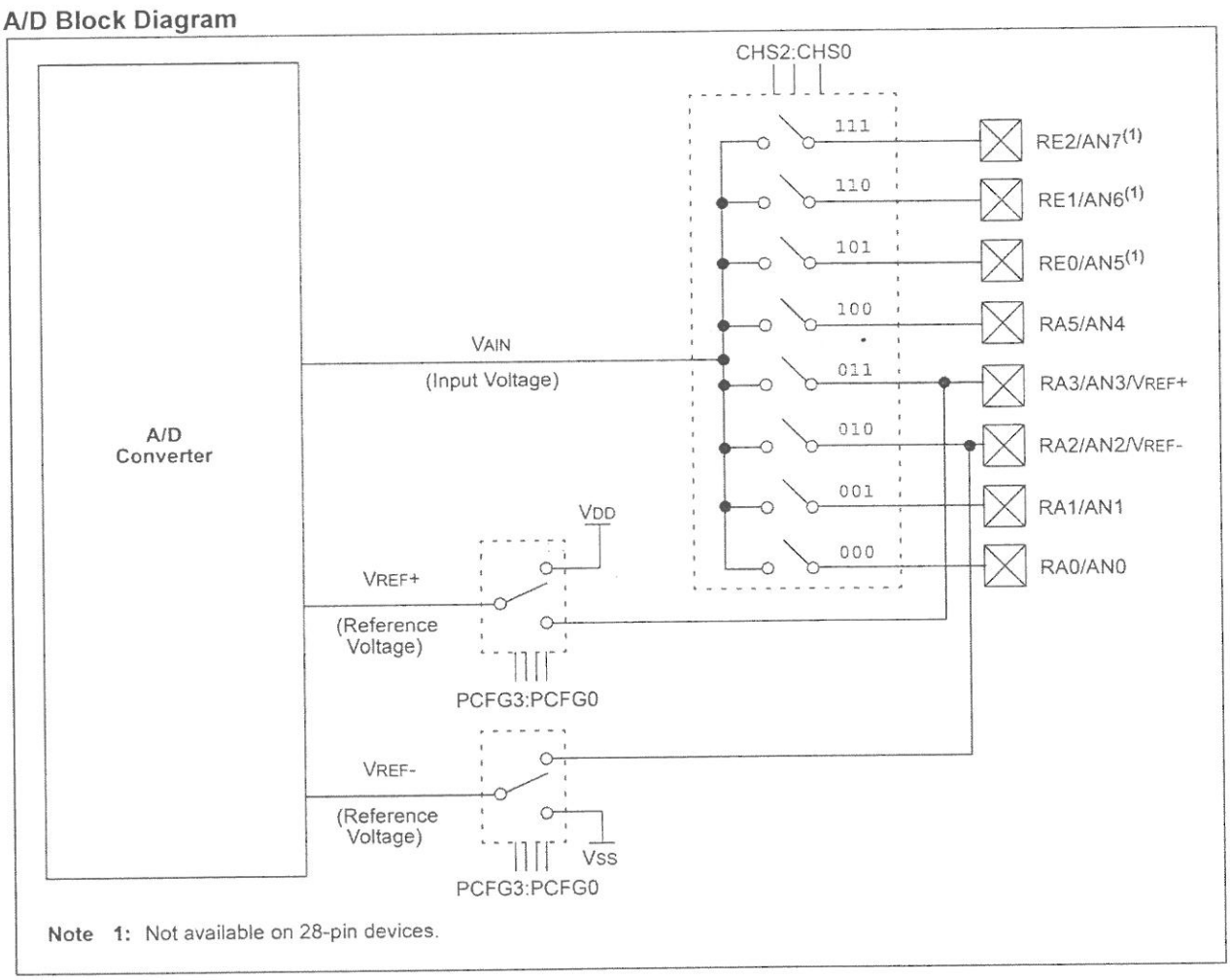

Figure 3(d)(i)

ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits

000 = Channel 0 (AN0)
001 = Channel 1 (AN1)
010 = Channel 2 (AN2)
011 = Channel 3 (AN3)
100 = Channel 4 (AN4)
101 = Channel 5 (AN5)
110 = Channel 6 (AN6)
111 = Channel 7 (AN7)

Note: The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Figure 3(d)(ii)

ADCON1: A/D CONTROL REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.

0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Note: On any device Reset, the port pins that are multiplexed with analog functions (ANx) are forced to be an analog input.

Figure 3(d)(iii)

Question 4

(a) A Timer 2 block diagram is shown in Figure 4(a). Timer 2 is used to generate a delay of 60μs.

(i) Determine the value of the PR2 if the TMR2 is 0, the prescaler and postscaler of 1:1 are selected. Assume that the crystal clock is running at the frequency of 16MHz. Ignore the overhead due to instructions in the calculation.

(5 marks)

(ii) Explain how the microcontroller knows the delay of 60μs has reached.

(3 marks)

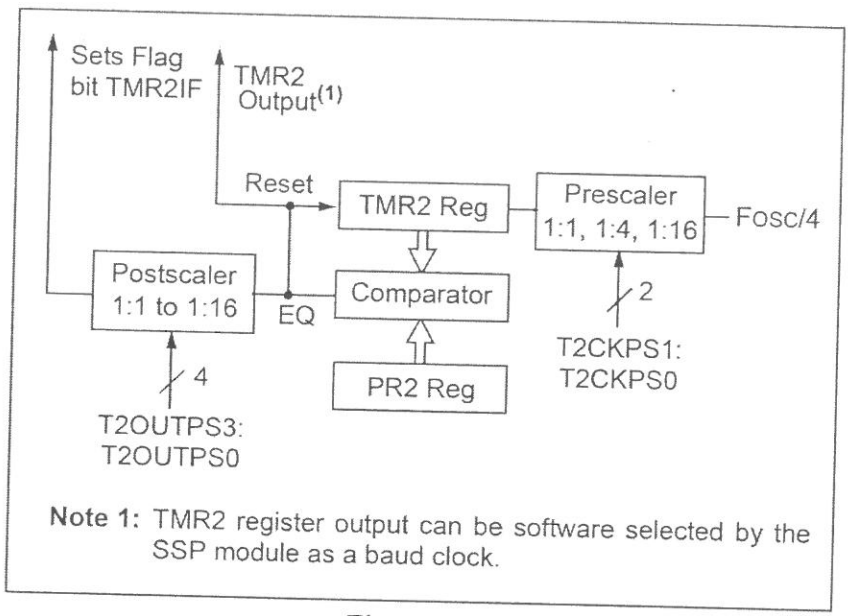

Figure 4(a)

(b) Define embedded system with an aid of the diagram. Label the diagram clearly.

(4 marks)

(c) Explain THREE (3) types of memories available in the Peripheral Interface Controller (PIC) microcontroller and how each of them are being used by the programmer.

(6 marks)

(d) Figure 4(d) shows the PIC to PIC communication via UART. Briefly explain the UART communication between these 2 PIC microcontrollers. Comment on the typical baud rate used for this communication. Assume the communication protocol used is 8N1. The figure below shows communication between two PIC16F877A microcontrollers.

(7 marks)

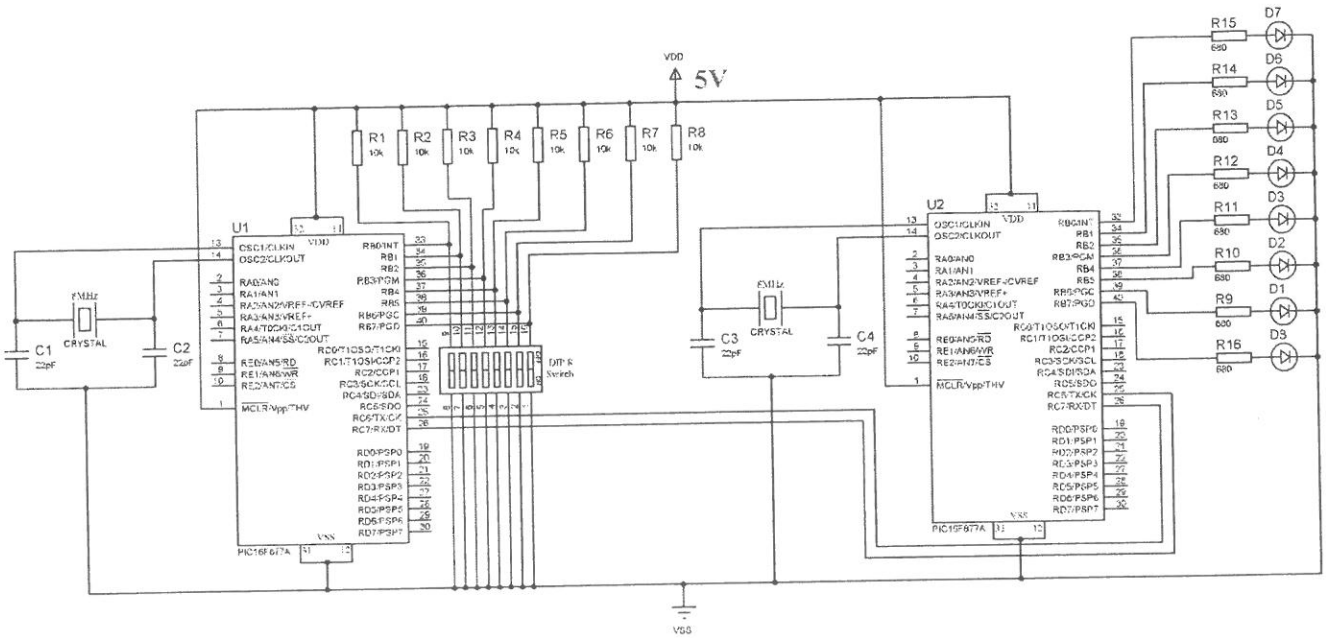

Figure 4(d)

Question 5

(a) Calculate the time delay subroutine taken for the Table 5(a) program which is running with the highest HS mode using 22 pF capacitors by the PIC16F877A microcontroller in Figure 5(a).

Include the instructions of `CALL DELAY` as well as `RETURN` into the calculation. Show all workings clearly as well as provide each instruction cycle time.

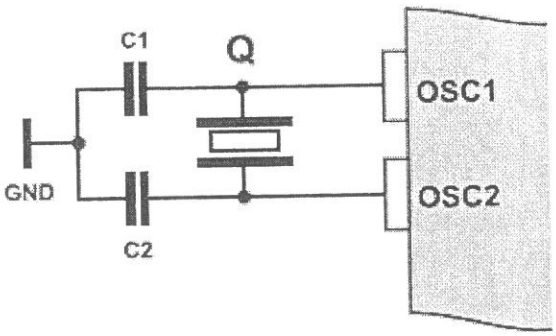

Figure 5(a)

Mode	Frequency	C1, C2
LP	32 KHz	33pF
	200 KHz	15pF
XT	200 KHz	47-68 pF
	1 MHz	15 pF
	4 MHz	15 pF
HS	4 MHz	15 pF
	8 MHz	15-33 pF
	20 MHz	15-33 pF

Program

```
DELAY:
        CLRF    0x20
        CLRF    0X30
AGAIN:  DECFSZ  0X30,1
        GOTO    AGAIN
        DECFSZ  0X20,1
        GOTO    $-4
        NOP
        CLRW
```

Table 5(a) Coding

(12 marks)

(b) Using the LED008 Alphanumeric LCD Display (16 × 2) datasheet provided in Appendix D, clearly differentiate between CGROM, CGRAM and DDRAM.

(6 marks)

Explain in details how a custom LCD display of Ω symbol shown in Figure 5(b) can be achieved using 5×7 dot matrix. Use diagram and program coding to aid your explanation.

(7 marks)

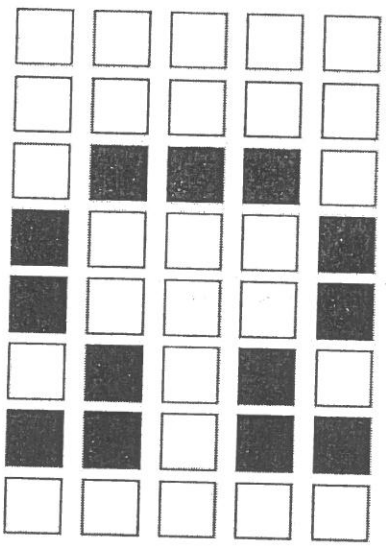

Figure 5(b)

Question 6

(a) Figure 6(a) shows a SST39SF040 multi-purpose flash memory chip pin configuration. This memory chip from Microchip will be used to connect with a PIC microcontroller externally. Determine the memory capacity in Kbits, memory organization and number of address pins and data pins used by this memory chip.

(6 marks)

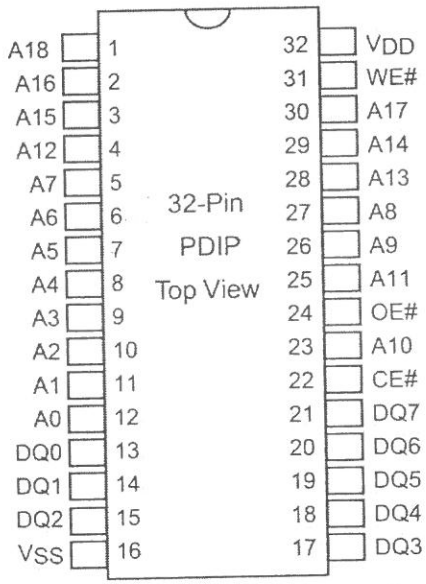

Figure 6(a) Flash Memory pin configuration

(b) What is major different between the Schmitt Trigger input and TTL input as shown in Table 6(b) for partial Port B Functions of PIC16F628A microcontroller?

(4 marks)

Name	Function	Input Type	Output Type	Description
RB0/INT	RB0	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up.
	INT	ST	—	External interrupt
RB1/RX/DT	RB1	TTL	CMOS	Bidirectional I/O port. Can be software programmed for internal weak pull-up.
	RX	ST	—	USART Receive Pin
	DT	ST	CMOS	Synchronous data I/O
RB2/TX/CK	RB2	TTL	CMOS	Bidirectional I/O port
	TX	—	CMOS	USART Transmit Pin
	CK	ST	CMOS	Synchronous Clock I/O. Can be software programmed for internal weak pull-up.

Table 6(b)

(c) Provide FIVE (5) main differences between microprocessor and microcontroller. Assuming cost and size of the chip are not the main differences.

(5 marks)

(d) Discuss the operation of both the von Neumann and Harvard architectures using appropriate diagrams to illustrate your answer. Clearly distinguish between them.

(5 marks)

(e) Provide FIVE (5) main differences between RISC and CISC processors.

(5 marks)

– THE END –

EEE2114(F)/Aug17/Steven Khoo/18/09/17