INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2017**
Programme	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE 2101: Introduction to Digital Electronics**
Date of Examination	:	14 December 2017 (Thursday)
Time	:	2:00pm – 4:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Worksheet 6(a) & Worksheet 6(b)

Examiner(s)	:	**Mr. Steven Khoo Boo Tap**
Moderator		Mr. Kevin Tan Geok Su

*This paper consists of **11** printed pages, including the cover page.*

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: AUG2017 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the letter 'bCdHInOrtU', respectively, as shown below in Figure 1(a-1). The BCD inputs are labelled as WXYZ, W is the MSB and Z is the LSB. Figure 1(a-2) shows a Common-Cathode 7 segment display. Assume all unused inputs as don't care.

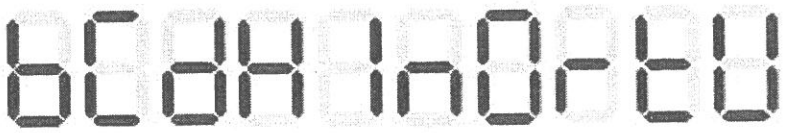

Figure 1(a-1)

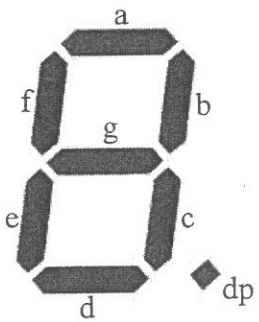

Figure 1(a-2)

(i) Develop the truth table for the inputs to segments a through g of the 7 segment. (4 marks)

(ii) Determine the SOP form of the logic expression for segments a, b and g. (6 marks)

(iii) Implement the logic expression using only 3-input NAND gate with minimum 7410 ICs consideration. State the number of ICs used. Show all working clearly. (7 marks)

(b) Using Boolean algebra and/or Karnaugh map, simplify to the following to simplest logic gate(s):

(i) where K is MSB and N is LSB.

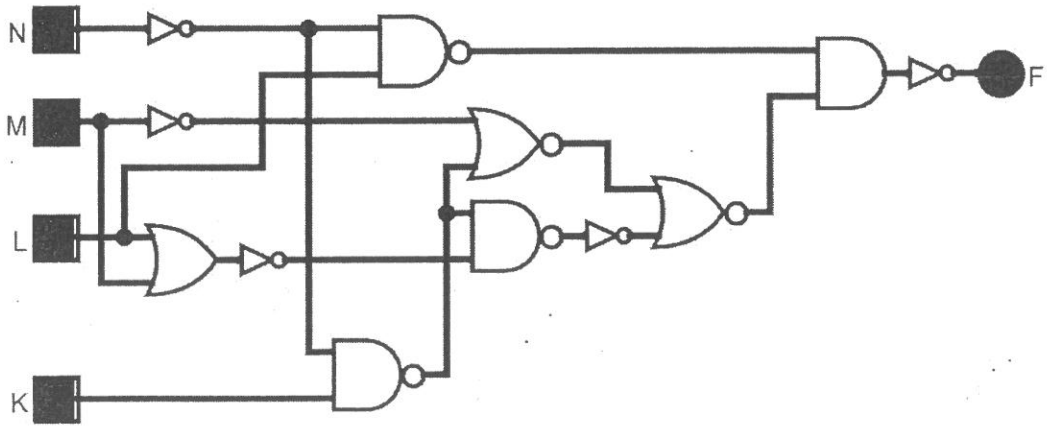

Figure 1(b)

(4 marks)

(ii) where A is MSB and C is LSB.

$Y = \overline{AC} \cdot \overline{ABC \cdot \bar{B}} + \bar{A} \cdot \bar{B} \cdot \bar{C}$

(4 marks)

Question 2

(a) Table 2(a) and Table 2(b) show a portion of a dual positive edge-triggered JK flip-flops (DM7476) and a triple 3-input AND gate datasheet respectively. Figure 2(a) show the logic circuit diagram of an asynchronous counter which uses positive edge-triggered JK flip-flops with labelling of $Q_A Q_B Q_C Q_D$ where Q_D is MSB and Q_A is LSB. Assume the environment is at $T_A = 25°C$ with $V_{CC} = 5V$.

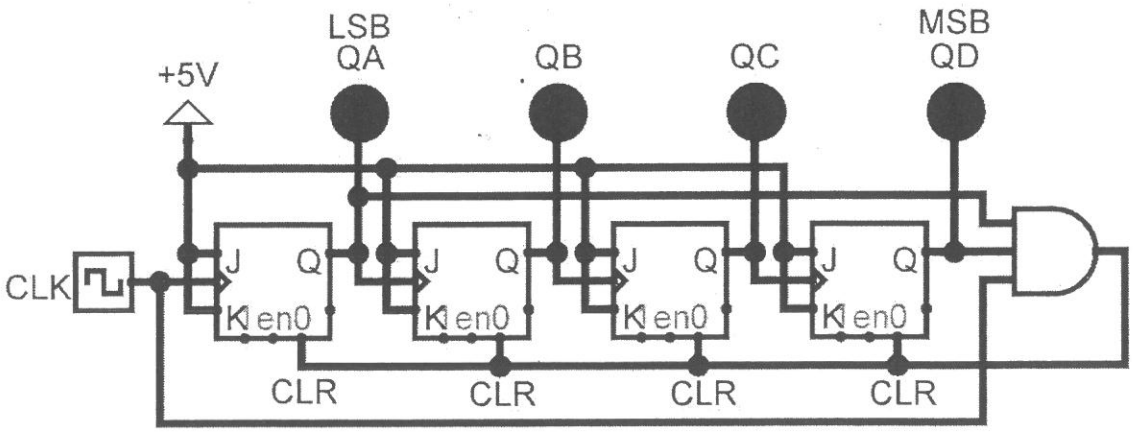

Figure 2(a)

Switching Characteristics
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25	ns

Table 2(a) JK flip-flop

Symbol	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B or C	Y	C_L = 15 pF, R_L = 2kΩ		8	27	ns
t_{PHL}					10	19	ns

Table 2(b) AND gate

(i) Analyse its operation to determine whether the logic circuit of Figure 2(a) is working or not. If not working, justify and suggest a suitable modification for the logic circuit to function as a counter.

(3 marks)

(ii) Determine total propagation delay from the given datasheets in Table 2(a) and Table 2(b).

(4 marks)

(iii) Determine the maximum frequency at which the counter can be operated stably.

(2 marks)

(iv) Show the output timing diagram of Figure 2(a) with proper labelling and state the exact function of this counter.

(4 marks)

(b) Perform the following number system transformation. Show all workings clearly.

(i) $[3016.3016_{16} - 1001.1001_{16}]$ to decimal equivalent with 5 decimal points accuracy.

(4 marks)

(ii) $[10215.01_8 \times 16_8]$ to hexadecimal equivalent with 3 hexadecimal points accuracy.
(4 marks)

(iii) $[163.0703125_{10} - 11.101_{16}]$ to binary equivalent with 12 binary points accuracy.
(4 marks)

Question 3

(a) Design a synchronous counter using positive edge-triggered JK flip-flop for MSB, D flip-flop for second bit, RS flip-flop for third bit and T flip-flop for LSB as shown in Figure 3(a). Assume J_A & K_A are the MSB inputs, D_B are the next flip-flop input, R_C & S_C are the next flip-flop inputs and T_D is the LSB input.

The counter sequence is as follow:
0 ⇨ 1 ⇨ 3 ⇨ 5 ⇨ 7 ⇨ 9 ⇨ 11 ⇨ 13 ⇨ 15 ⇨ 14 ⇨ 12 ⇨ 10 ⇨ 8 ⇨ 6 ⇨ 4 ⇨ 2 ⇨ 0.
Use $Q_AQ_BQ_CQ_D$ outputs labelling for J_A & K_A, D_B, R_C & S_C and T_D inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.

(i) Provide the excitation table used and the state diagram.
(4 marks)

(ii) Provide the transition table/ next state table.
(4 marks)

(iii) Simplify using Karnaugh map and Boolean algebra if necessary.
(6 marks)

(iv) Draw the complete logic circuit diagram with proper label.
(5 marks)

For example, the output sequence of 5 or $Q_AQ_BQ_CQ_D$ equals to 0101.

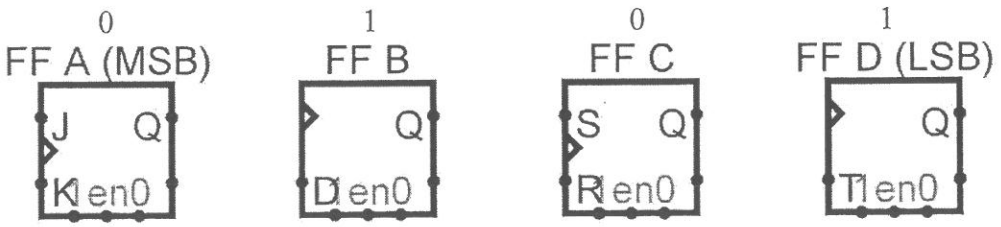

Figure 3(a)

(b) An S-R latch is driven from a 2-bit binary counter with outputs designated B1B0 (B1 is the MSB). Output B1 is ANDed with $B1 \oplus B0$ and drives the R input to the latch. B0 is also ANDed with $B1 \oplus B0$ and drives S as shown in Figure 3(b) below.

(i) Draw the logic circuit showing the inputs, B1 & B0 and output, Q of SR latch.
(3 marks)

(ii) Construct a table to record the output, Q of the S-R latch as the counter steps through its 4 states beginning with B1B0 = 00. Assume the output is initially RESET.
(3 marks)

Question 4

(a) For the pulse shown in Figure 4(a) below, graphically determine the Rise time, Fall time, Pulse time and Amplitude.

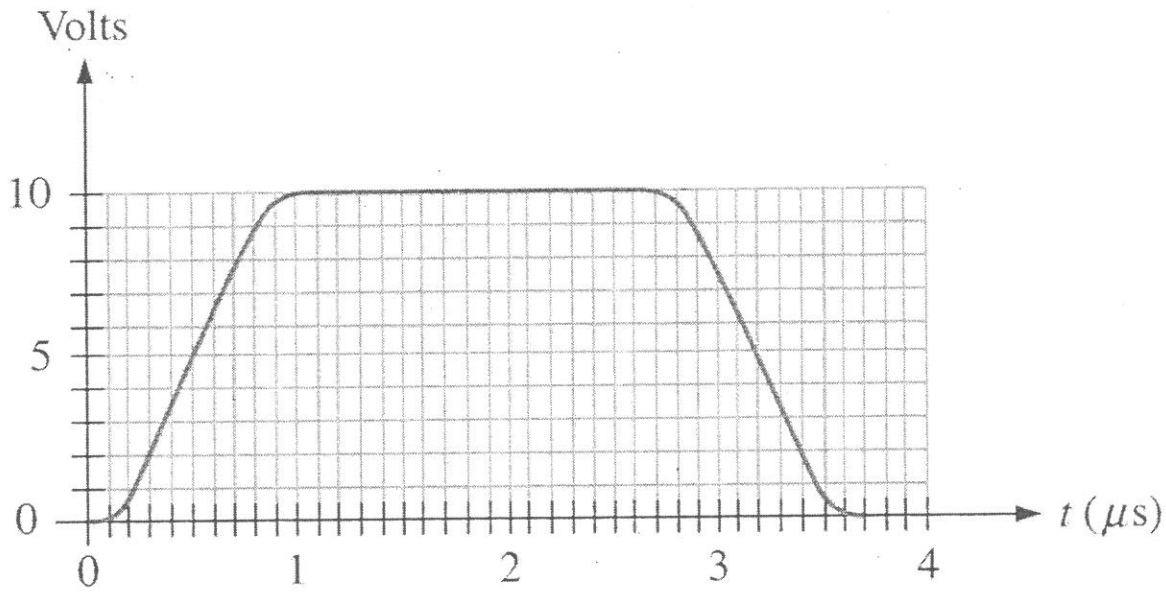

Figure 4(a)

(4 marks)

(b) Figure 4(b) below shows a 4-bit synchronous counter which is designed so that it performs a special counting sequence. Analyse its operation by determining its counting sequence. Assume that all flip-flops are initially in the 0 state (0000) for $Q_3Q_2Q_1Q_0$. Flip-flop FF3 is MSB and FF0 is LSB. Use J_3K_3, J_2K_2, J_1K_1 and J_0K_0 inputs labelling for Q_3, Q_2, Q_1 and Q_0 outputs. Show all workings clearly.

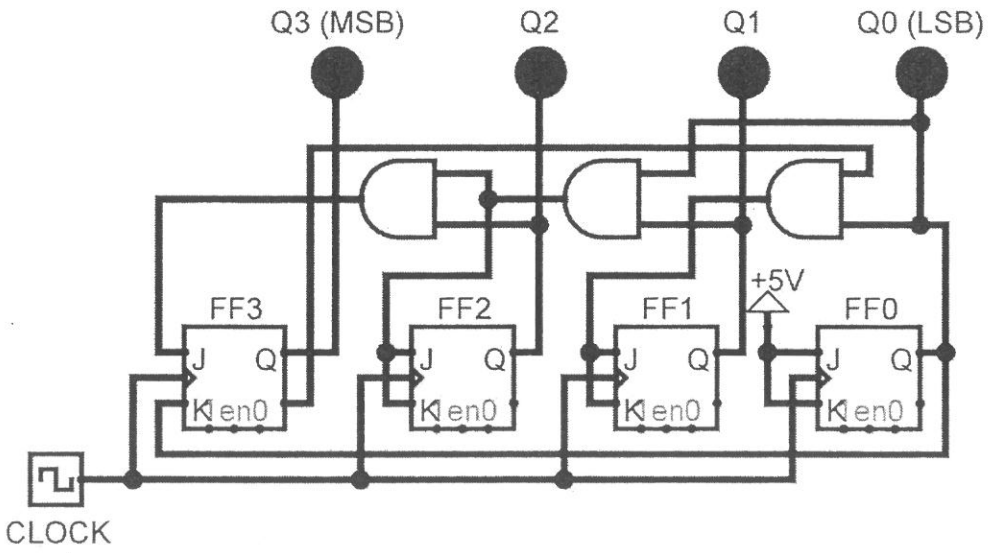

Figure 4(b)

(i) Provide the Boolean expressions from the logic circuit.

(3 marks)

(ii) Provide all Karnaugh maps according to the expressions.

(4 marks)

(iii) Provide the transition table/ next state table with excitation table.

(5 marks)

(iv) Draw the state diagram and comment on the outcome of the states obtained.

(3 marks)

(c) A binary-weighted-input DAC is shown in Figure 4(c). If the LSB bit resistor has a value of 480kΩ, compute the values of the other input resistors. Also, calculate the V_{out} if the DAC has a binary input of 1011 with Logic 1 (HIGH) as +5.0V and Logic 0 (LOW) as 0V. Assume that R_f equals to 12kΩ. What are the disadvantages of this method of DAC?

(6 marks)

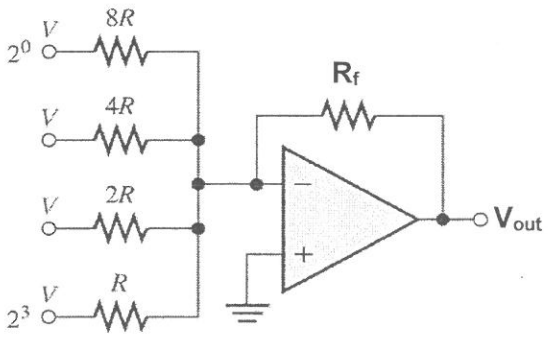

Figure 4(c)

Question 5

(a) Implement the function using an appropriate multiplexer (MUX) with other logic gates, taking into consideration of minimum gates count as well.

(i) $F_1(R,S,T,U) = \sum(3,4,6,7,8,10,12,14)$ with RT as the select lines.

(4 marks)

(ii) $F_2(W,X,Y,Z) = \sum(0,2,5,6,10,11,12,15)$ with X as the select line.

(4 marks)

(b) Figure 5(b) represents an adder circuit that takes two-bit binary numbers X_1X_0 and Y_1Y_0 and produces an output binary number Z_1Z_0 and Carry that is equal to the arithmetic addition of the two input numbers.

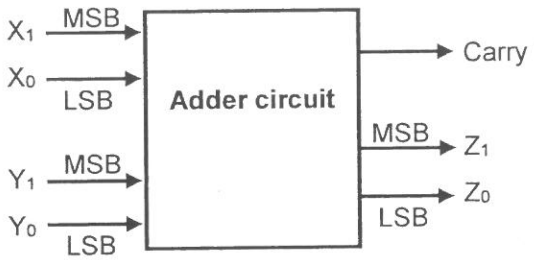

Figure 5(b)

Design the logic circuit for the adder. Show all working clearly. Hint: The logic circuit will have four inputs and three outputs as shown in Table 5(b).

(i) Complete the truth table below.

Input X		Input Y		Output Z		Carry
X_1	X_0	Y_1	Y_0	Z_1	Z_0	
0	0	0	0	0	0	0
0	0	0	1	0	1	0
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	0	0	1	1
1	1	1	1	1	0	1

Table 5(b)

(3 marks)

(ii) Simplify the Boolean expression to the simplest form using Karnaugh map and/or Boolean algebra for output Z_1, Z_0 and Carry.

(9 marks)

(iii) Implement the logic circuit of the simplest Boolean expression for Z_0 using only 2-input NAND gate IC (7400). State the number of IC(s) required for your design.

(5 marks)

Question 6

(a) A T flip-flop is connected as shown below in Figure 6(a)(i). Determine the output, Q with the given input, Y waveform as shown below in Figure 6(a)(ii). The Q is initially at LOW. Assume that there is no propagation delay issue and the flip-flop has been enabled.

Note: Use **Worksheet 6(a)** to answer this question and tie with the answer script.

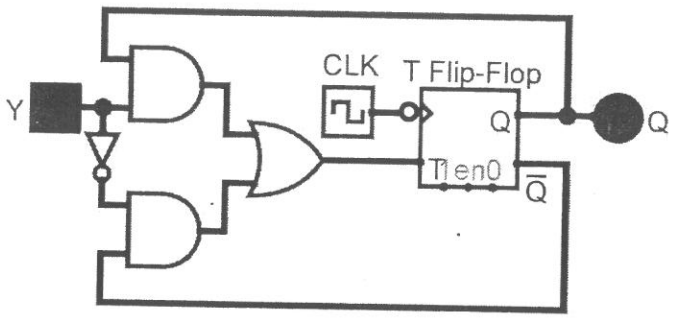

Figure 6(a)(i)

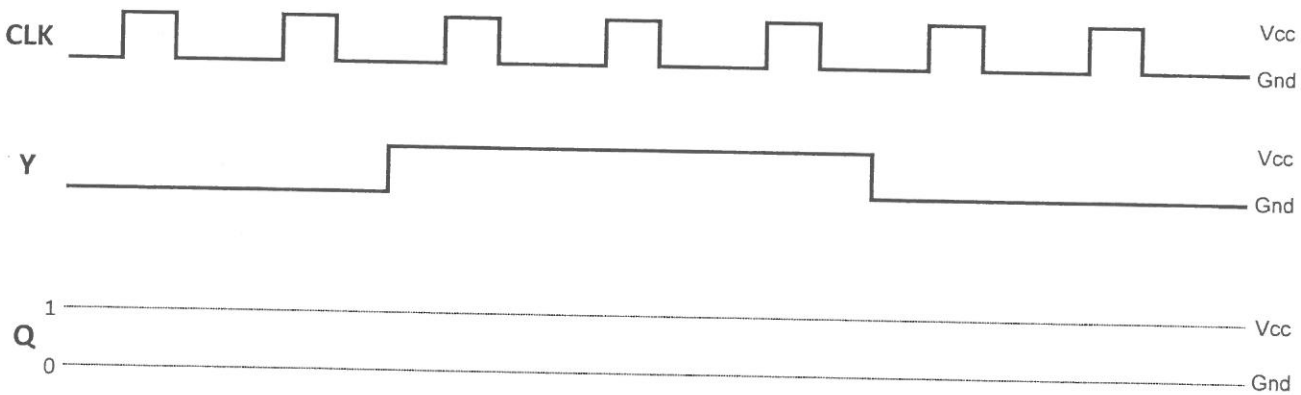

Figure 6(a)(ii)

(5 marks)

(b) A D flip-flop is connected as shown below in Figure 6(b)(i). Determine the output, Q with the given inputs, A and B waveforms as shown in Figure 6(b)(ii). The Q is initially at HIGH. Assume that there is no propagation delay issue and the flip-flop has been enabled.

Note: Use **Worksheet 6(b)** to answer this question and tie with the answer script.

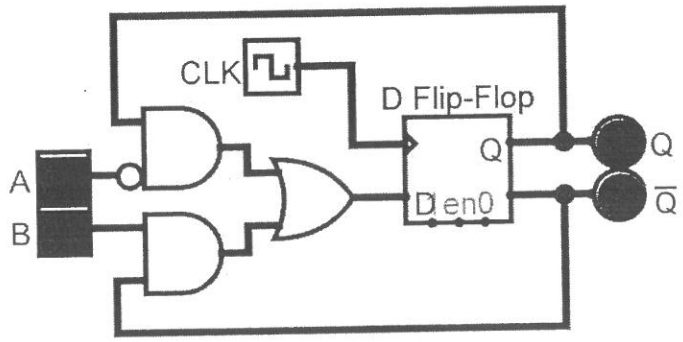

Figure 6(b)(i)

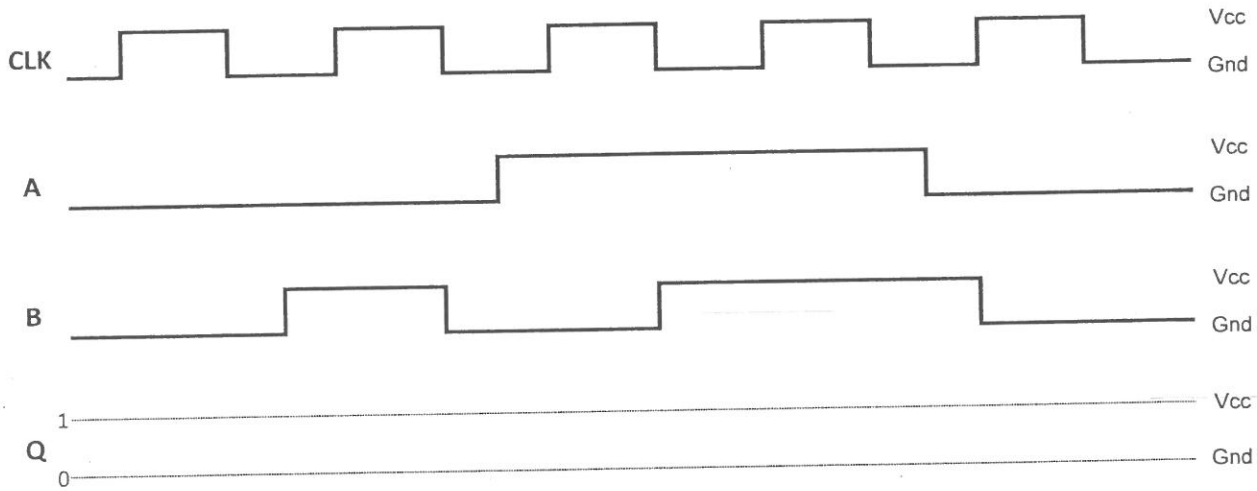

Figure 6(b)(ii)

(5 marks)

(c) A 12-bit DAC produces an output current in proportion to its digital input. For a digital input of 000010100000, an output current of 75mA is produced.

(i) What will the output current be if the digital input is 100100011110?

(3 marks)

(ii) What is the maximum output current produced by this DAC?

(2 marks)

(iii) What should the digital input be if a 1205mA output current is required?

(2 marks)

(d) Table 6(d) shows the current ratings of TTL series logic gates. A 74AS08 AND gate output is driving 4 (FOUR) Standard TTL gate inputs, 2 (TWO) Advanced Low-Power Schottky gate inputs and 14 (FOURTEEN) Low-Power Schottky gate inputs. Determine if there is a loading problem.

(4 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

Table 6(d)

The 74AS08 AND gate output needs to be used to drive some 74F inputs in addition to the load inputs. How many additional 74F inputs could the output drive without being overloaded?

(4 marks)

– THE END –

EEE2101(F)/Aug17/Steven Khoo/16/09/17

Worksheet 6(a)

(a) A T flip-flop is connected as shown below in Figure 6(a)(i). Determine the output, Q with the given input, Y waveform as shown below in Figure 6(a)(ii). The Q is initially at LOW. Assume that there is no propagation delay issue and the flip-flop has been enabled.

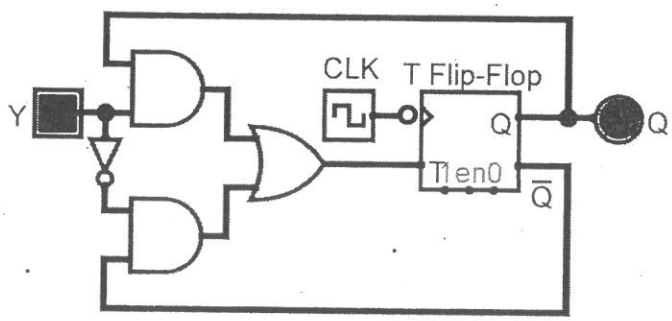

Figure 6(a)(i)

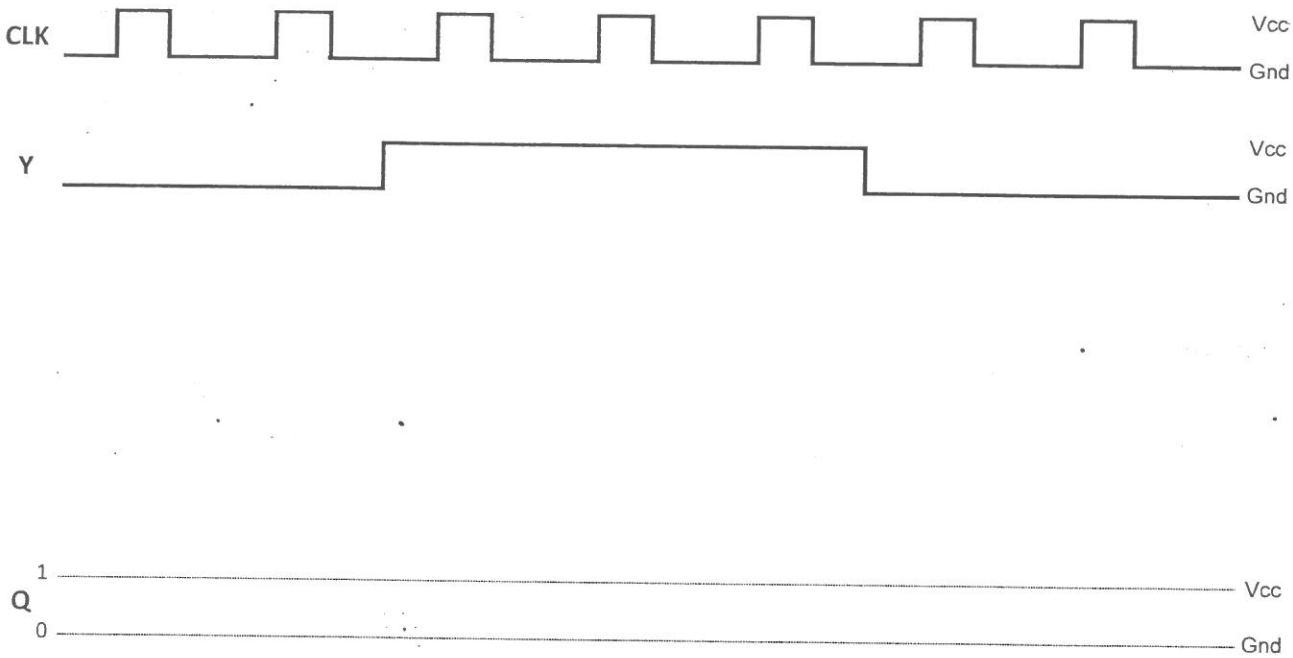

Figure 6(a)(ii)

(5 marks)

Worksheet 6(b)

(b) A D flip-flop is connected as shown below in Figure 6(b)(i). Determine the output, Q with the given inputs, A and B waveforms as shown in Figure 6(b)(ii). The Q is initially at HIGH. Assume that there is no propagation delay issue and the flip-flop has been enabled.

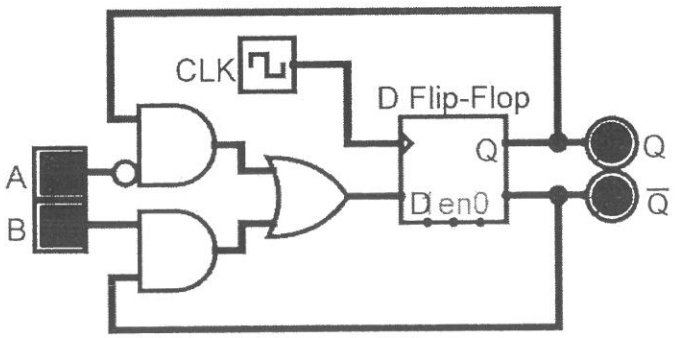

Figure 6(b)(i)

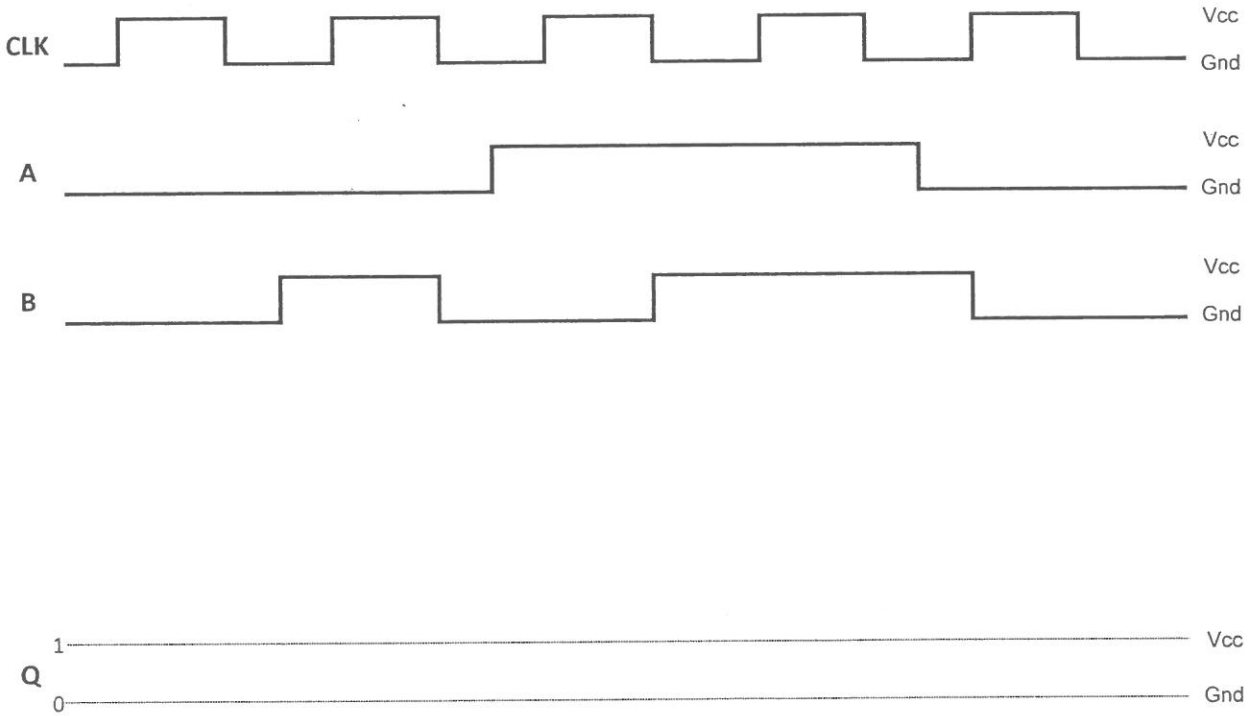

Figure 6(b)(ii)

(5 marks)