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International College Penang
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FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2017**
Programmes	:	Diploma in Electrical and Electronic Engineering (DEEI)
Course	:	**EEE1106: Analogue Electronics**
Date of Examination	:	12 December 2017 (Tuesday)
Time	:	11:00am – 1:00pm
Duration	:	2 Hours Reading Time Nil
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : **THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.**

Materials Permitted :
Scientific Calculator (Model fx570 Series)

Materials Provided :
Nil

Examiner(s)	:	**Chan Tse Wei**
Moderator	:	Assoc. Prof. Dr. Khoo Bee Ee

This paper consists of 8 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1106: ANALOGUE ELECTRONICS
FINAL EXAMINATIONS: AUGUST 2017 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. Present your answers neatly and clearly. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

a. Figure-Q1(a) shows the frequency response plot of a single stage AC-coupled common source amplifier evaluated with input voltages having fixed 1 V amplitude. The amplifier output is terminated with a pure resistive load.

i. Estimate the mid-band voltage gain of the amplifier in dB. [4]

ii. Explain the root causes of the output voltage reduction exhibited at both ends of the frequency response plot. [4]

iii. Estimate the bandwidth of the amplifier. [4]

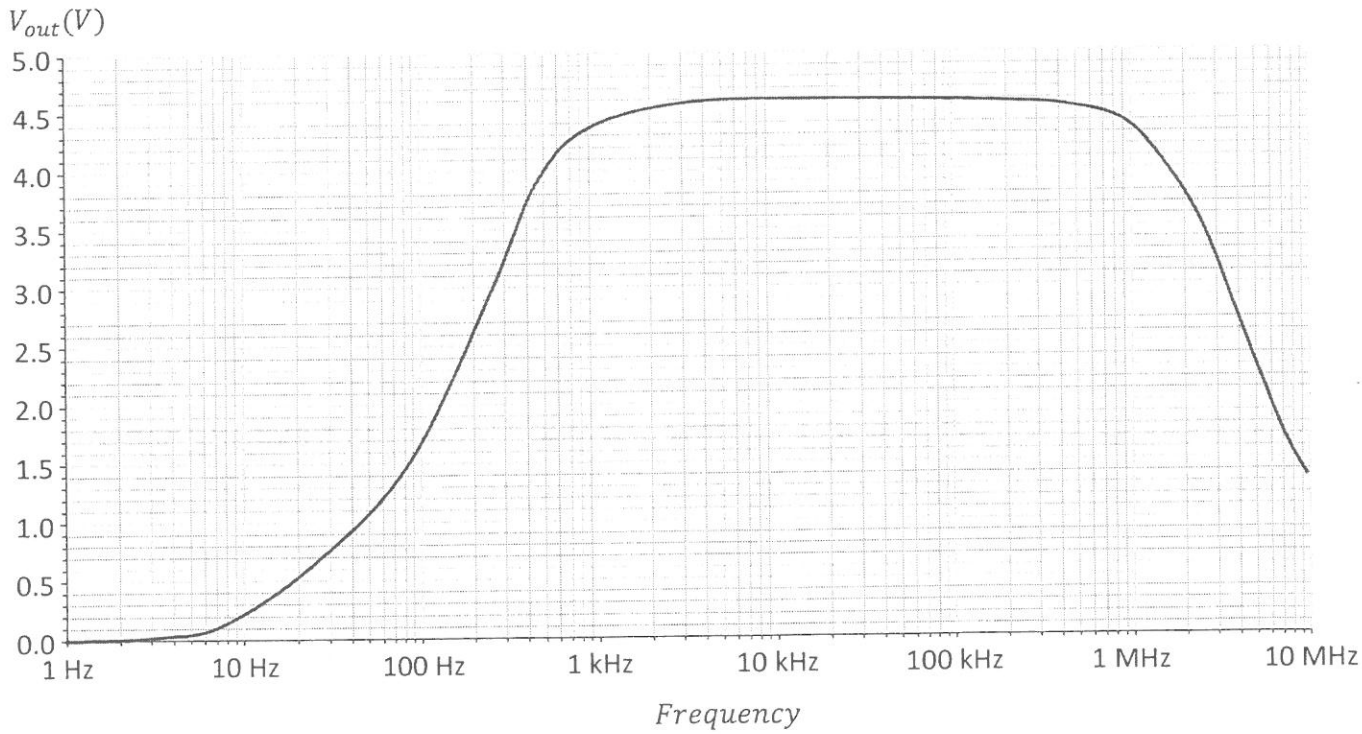

Figure-Q1(a)

b. Figure-Q1(b) shows a JFET-based voltage amplifier. Experiment results reveal the amplifier has a maximum voltage gain, v_{out}/v_{in} of 14 dB. Use this information to estimate the transconductance (g_m) of the JFET. State any assumption made in your estimation and show all workings clearly. [13]

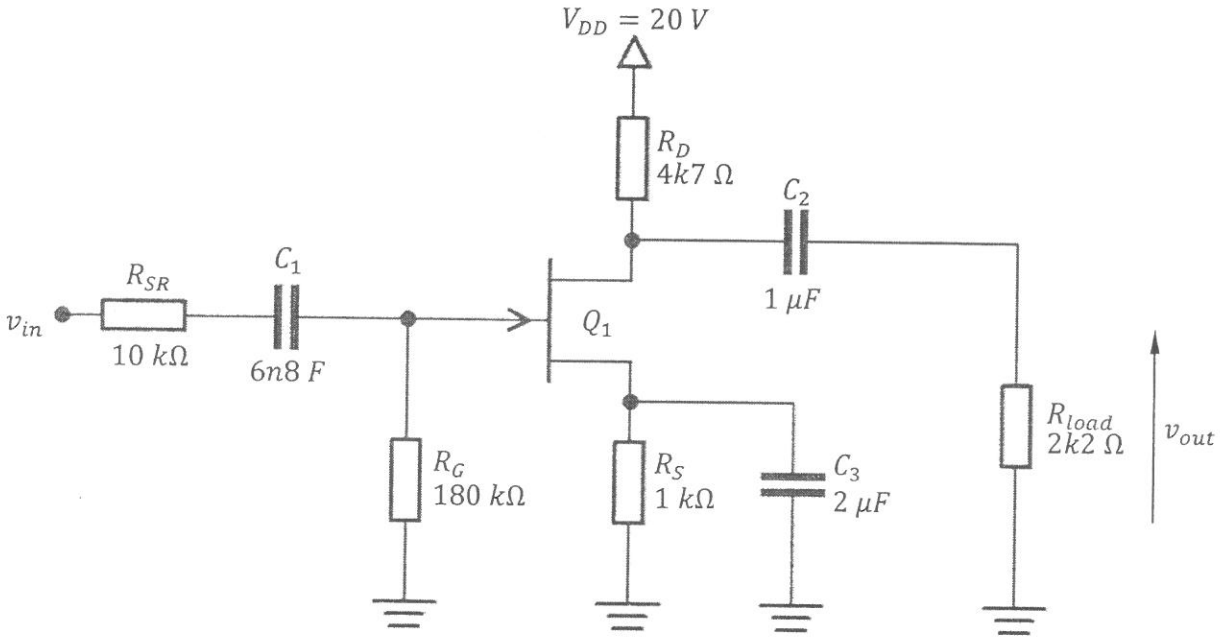

Figure-Q1(b)

Question 2

a. Figure-Q2(a)(i) shows a power amplifier circuit. Evaluation results reveal that the amplifier has the following DC operating points:

$$V_{B_Q} = 0.48\ V$$

$$V_{C_Q} = 7.30\ V$$

Figure-Q2(a)(ii) shows the waveforms measured at port v_{in}, $V(vin)$ and the output voltage across resistor R_{load}, $V(VCC, VC)$.

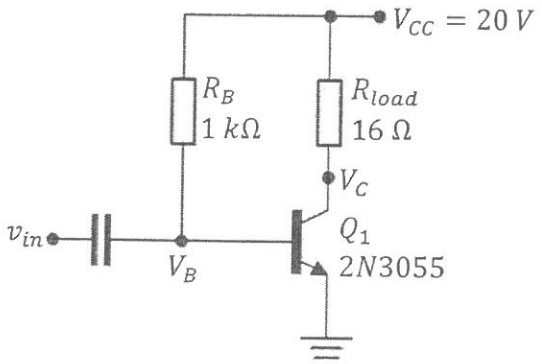

Figure-Q2(a)(i)

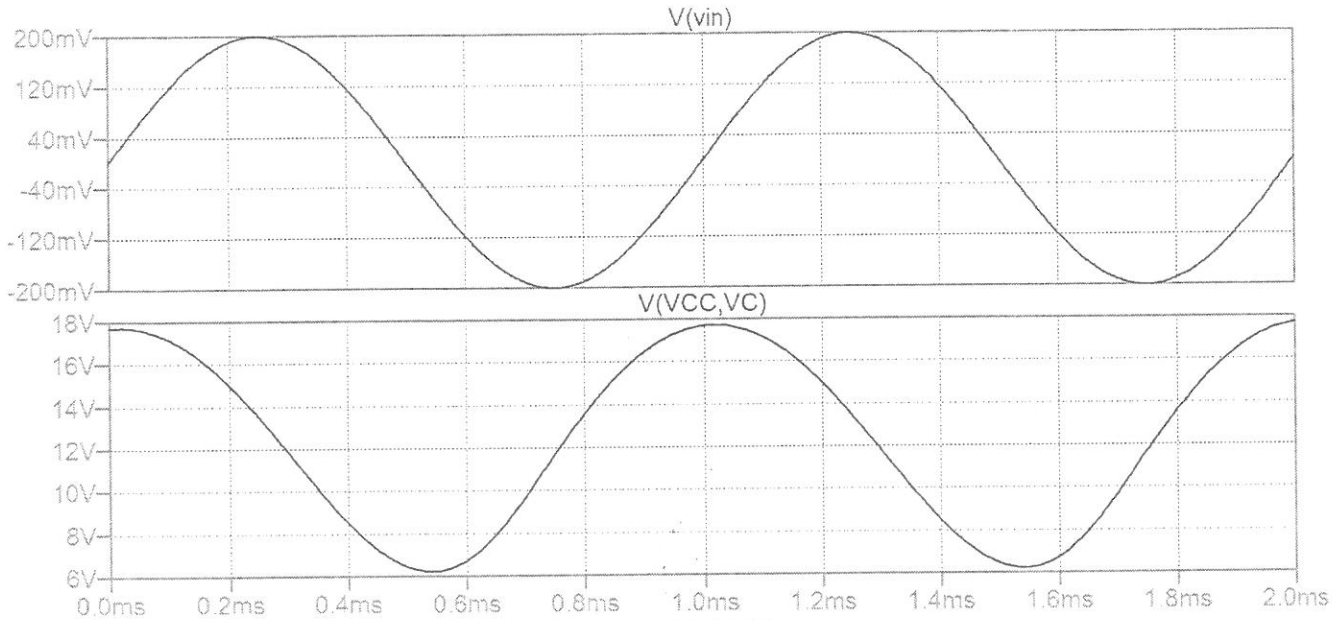

Figure-Q2(a)(ii)

i. Identify the class of the power amplifier in Figure-Q2(a)(i). [2]

ii. Calculate the total DC power, P_{DC}, applied to the amplifier. [6]

iii. Calculate the estimated total AC power, P_{AC}, delivered to load R_{load} by the amplifier. [5]

iv. Calculate the power efficiency of the amplifier. [2]

v. State one advantage and one disadvantage of this type of power amplifier. [2]

b. A class B power amplifier using common collector configuration, has a $\pm 25\ V$ supply voltage, while its load resistance is 16 Ω. A 20 V peak input AC voltage is supplied to this power amplifier. Assume ideal transistor operation, calculate

i. its total input DC power, P_{DC}. [4]

ii. its output AC power, P_{AC}. [2]

iii. its power conversion efficiency in percentage. [2]

Question 3

a. i. Most op-amps are powered in a dual supply mode. Explain the principal advantage to do so. [3]

ii. State the output voltage expression of an op-amp, in terms of its two input voltages, V^+ and V^-, and its open-loop voltage gain, A_o. [2]

iii. Explain output voltage saturation limit of an op-amp. [3]

iv. Sketch the idealized voltage transfer characteristic, V_{out} versus $(V^+ - V^-)$, of an op-amp clearly. [3]

b. For each of the following statement, state TRUE or FALSE.

i. In ideal open-loop op-amp operation, the slightest non-zero value of $(V^+ - V^-)$ will drive its output voltage to saturation. [1]

ii. When the output voltage of an op-amp lies between its power supply voltages, the op-amp is said to be operating in its saturation region. [1]

iii. The input resistance of an op-amp is designed to be as low as possible so that negligible power dissipates in the op-amp. [1]

iv. Applying negative feedback to an op-amp helps to reduce the overall voltage gain of the op-amp circuit. [1]

v. Positive feedback should be entirely avoided in op-amp circuit design. [1]

c. i. Design an op-amp circuit to implement the block diagram shown in Figure-Q3(c). [5]

ii. Clearly sketch the idealized voltage transfer curve of the circuit. [4]

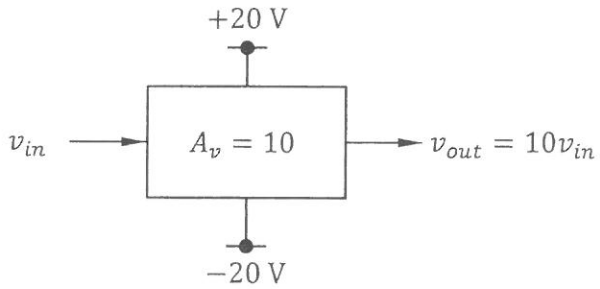

Figure-Q3(c)

Question 4

Figure-Q4 shows an active band pass filter adopting multiple feedback topology. The general voltage transfer function expression of the filter is given by,

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{a_1 s}{s^2 + \left(\frac{\omega_o}{Q}\right)s + \omega_o^2}$$

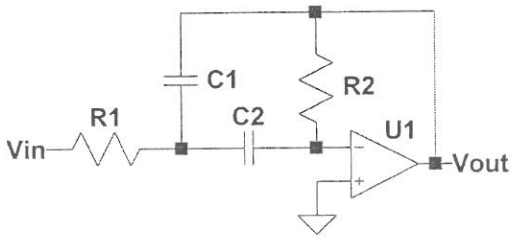

Figure-Q4

a. Explain the significant meaning of the negative sign shown in the given voltage transfer function expression. [2]

b. Explain the meaning of the symbol "Q" and "ω_o" shown in the given voltage transfer function expression. [4]

c. Relate "a_1", "Q" and "ω_o" to the passive components used in the filter. [10]

d. By choosing $C_1 = 1\ nF$, determine the values for the remaining passive components so that the filter has a bandwidth of 4 kHz and a maximum voltage gain of 10 at 5 kHz. [9]

Question 5

a. Figure-Q5(a)(i) shows a block diagram of an oscillator. Symbol A_v and β respectively represent the amplifier voltage gain and the system's feedback factor. Figure-Q5(a)(ii) shows the output signal of the oscillator, measured when the circuit is first powered up.

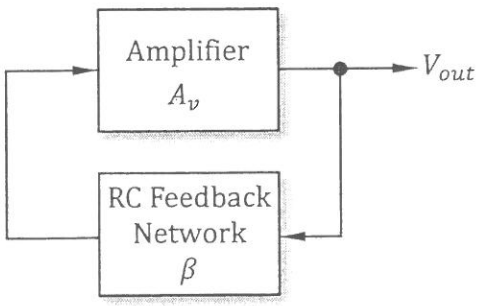

Figure-Q5(a)(i)

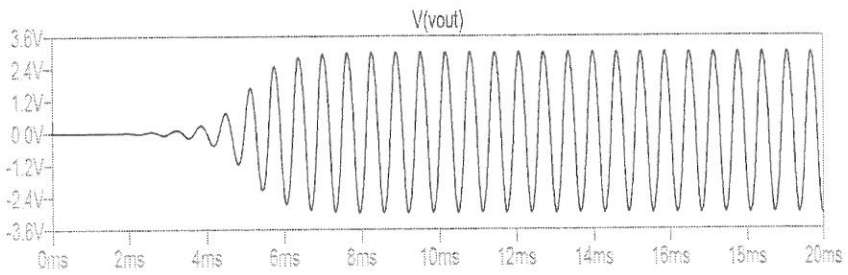

Figure-Q5(a)(ii)

i. State the family of the oscillator given in Figure-Q5(a)(i). [2]

ii. Relate A_v and β for $t < 6\,ms$. [2]

iii. Relate A_v and β for $t > 8\,ms$. [2]

iv. State two existing examples of oscillator circuit that are built base on the configuration given in Figure-Q5(a)(i). [2]

b. Figure-Q5(b) shows an oscillator circuit which implements the circuit configuration as shown in Figure-Q5(a)(i). The circuit is at its steady-state condition.

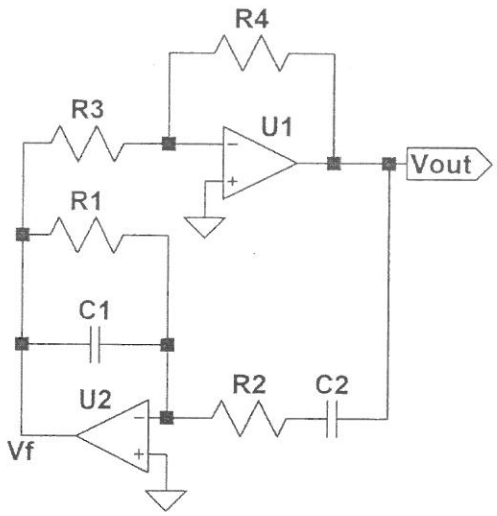

Figure-Q5(b)

i. By making use of the feedback network in Figure-Q5(b), show that output oscillating frequency of the circuit, in rad/s, is given by,

$$\omega_o = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}}$$ [6]

ii. Show that, during steady-state, the magnitude expression of the voltage amplifier's gain, $|A_v|$, is given by,

$$|A_v| = \frac{C_1}{C_2} + \frac{R_2}{R_1}$$ [5]

iii. Using as many equal-value components as possible, implement the circuit in Figure-Q5(b) to produce a signal oscillating with 5 kHz at steady-state condition. [6]

Question 6

a. Figure-Q6(a) shows a common emitter amplifier circuit. Transistor Q_1 has the following values of hybrid parameters under its small-signal operating conditions: $h_{ie} = 1\ k\Omega$, $h_{fe} = 100$, h_{oe} and h_{re} are negligible.

The amplifier has a voltage gain, $A_v = \frac{v_{out}}{v_{in}} = -10$ at frequency where the reactances of both C_1 and C_2 are negligible.

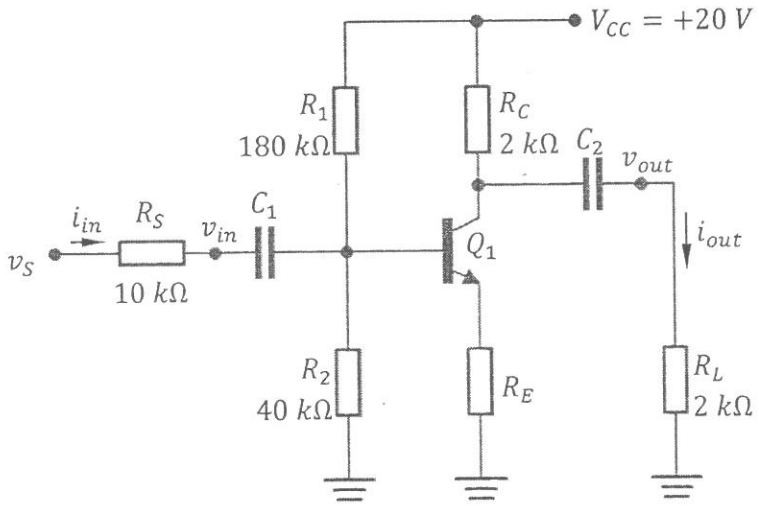

Figure-Q6(a)

i. Draw the equivalent AC circuit model of the given amplifier in which its voltage gain, $A_v = -10$. [4]

ii. Calculate the required value of R_E. [5]

iii. Calculate the current gain, $A_i = \frac{i_{out}}{i_{in}}$. [6]

b. i. State one advantage of a Schmitt Trigger Comparator as compared to an ordinary comparator circuit utilizing only an op-amp and one reference voltage. [2]

ii. Draw a non-inverting Schmitt Trigger Comparator that has positive upper and lower threshold points. The comparator is to be operated in single supply mode. [4]

iii. Design the circuit with threshold points set at 0.5 V and 2.5 V respectively, assume that the op-amp output saturates at 0V and 5V. [4]

~ The End ~