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INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session : AUGUST 2016

Programme : DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING

Course : EEE2114: INTRODUCTION TO EMBEDDED SYSTEMS

Date of Examination : 8 December 2016 (Thursday)

Time : 2:00pm – 4:00pm Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Appendix booklet (Please do not write anything on it)

Examiner(s) : **Steven Khoo Boo Tap**

Moderator : **Kevin Tan Geok Su**

This paper consists of 12 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2114: INTRODUCTION TO EMBEDDED SYSTEMS
FINAL EXAMINATION: AUG2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Figure 1(a) below shows the Port A Functions of PIC16F628A microcontroller. Explain how the pin RA4 and pin RA5 of PIC16F628A microcontroller can be used as output function; otherwise provide the reason why it can't. Use appropriate circuit diagram to aid your explanation.

(7 marks)

Name	Function	Input Type	Output Type	Description
RA0/AN0	RA0	ST	CMOS	Bidirectional I/O port
	AN0	AN	—	Analog comparator input
RA1/AN1	RA1	ST	CMOS	Bidirectional I/O port
	AN1	AN	—	Analog comparator input
RA2/AN2/VREF	RA2	ST	CMOS	Bidirectional I/O port
	AN2	AN	—	Analog comparator input
	VREF	—	AN	VREF output
RA3/AN3/CMP1	RA3	ST	CMOS	Bidirectional I/O port
	AN3	AN	—	Analog comparator input
	CMP1	—	CMOS	Comparator 1 output
RA4/T0CKI/CMP2	RA4	ST	OD	Bidirectional I/O port. Output is open drain type.
	T0CKI	ST	—	External clock input for TMR0 or comparator output
	CMP2	—	OD	Comparator 2 output
RA5/$\overline{MCLR}$/VPP	RA5	ST	—	Input port
	$\overline{MCLR}$	ST	—	Master clear. When configured as $\overline{MCLR}$, this pin is an active low Reset to the device. Voltage on $\overline{MCLR}$/VPP must not exceed VDD during normal device operation.
	VPP	HV	—	Programming voltage input.
RA6/OSC2/CLKOUT	RA6	ST	CMOS	Bidirectional I/O port
	OSC2	—	XTAL	Oscillator crystal output. Connects to crystal resonator in Crystal Oscillator mode.
	CLKOUT	—	CMOS	In RC or INTOSC mode, OSC2 pin can output CLKOUT, which has 1/4 the frequency of OSC1
RA7/OSC1/CLKIN	RA7	ST	CMOS	Bidirectional I/O port
	OSC1	XTAL	—	Oscillator crystal input. Connects to crystal resonator in Crystal Oscillator mode.
	CLKIN	ST	—	External clock source input. RC biasing pin.

Legend: O = Output, — = Not used, TTL = TTL Input, CMOS = CMOS Output, I = Input, OD = Open Drain Output, P = Power, ST = Schmitt Trigger Input, AN = Analog

Figure 1(a)

(b) Discuss the operation of both the Von Neumann and Harvard computer structures using appropriate diagram to illustrate your answer. Clearly distinguish between them.

(4 marks)

(c) Provide FOUR (4) main differences between RISC and CISC processors.

(4 marks)

(d) Explain THREE (3) types of memories available in the Peripheral Interface Controller (PIC) and the role played by each of them.

(6 marks)

(e) Provide FOUR (4) main differences between microprocessor and microcontroller.

(4 marks)

Question 2

(a) Given the Special Function Registers and File Registers as follows:

Table 2(a)(i) Special Function Registers

Update	Address	Symbol Name	Value
		WREG	32
	003	STATUS	00011001
	004	FSR	176
	006	PORTB	0X00
	00E	TMR1	0x0000
	011	TMR2	0x20
	086	TRISB	11111111

Table 2(a)(ii) File Registers

Address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
000	--	00	00	19	B0	00	00	--	--	--	16	77	00	--	00	00
010	20	00	00	--	--	00	55	33	60	00	00	--	--	--	--	00
020	61	12	10	56	34	18	52	AA	11	33	22	44	50	60	78	80
030	14	24	34	45	54	64	74	84	94	A4	B4	C4	D4	E4	F4	04
040	21	31	41	51	62	71	81	91	01	02	03	04	05	06	07	08
050	09	0A	0B	0C	0D	E0	0E	0F	F0	35	36	37	38	39	40	42
060	42	46	47	48	49	56	85	57	58	59	5A	5B	5C	5D	5E	5F
070	63	65	66	67	68	69	6A	6B	6C	6D	6E	6F	72	73	74	75
080	--	FF	00	18	20	FF	FF	--	--	--	16	77	70	--	08	--
090	--	--	FF	--	--	--	--	--	02	79	7A	7B	0C	00	--	6E
0A0	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	92	93
0B0	94	95	96	97	98	99	9A	9B	9C	9D	9F	9E	A0	B0	C0	D0
0C0	E0	F0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AD	AE
0D0	00	0A	44	00	00	00	00	00	00	00	00	00	00	00	00	00
0E0	00	1C	00	00	00	00	00	00	00	00	00	00	00	00	00	00
0F0	00	00	00	00	35	00	00	00	00	00	00	00	00	00	00	00

Perform the following operations. Indicate the result of the affected register(s) and Status (Z, DC and C). The operations are independent of each other. Show all workings of before and after with appropriate diagram illustration.

```
(i)    XORWF     FSR, W
(ii)   RRF       INDF, 2
(iii)  IORWF     INDF, F
(iv)   COMF      0x35, 1
(v)    SUBWF     INDF, 3
(vi)   SWAPF     0x23, 0
```

(18 marks)

(b) Assume that a 1-second delay subroutine for the PIC16F628A microcontroller is available and named as DELAY1S. Write a subroutine program that will produce a 1-minute delay instead. Include comments for all instructions used.

(7 marks)

Question 3

(a) Figure 3(a) below shows the Port B Functions of PIC16F877A microcontroller. Pin RB4:RB7 of PIC16F877A are normally used in keypad interfacing, explain why? Sketch the circuit diagram connection of Port B of PIC16F877A microcontroller and the 4 × 4 matrix keypad.

(8 marks)

Name	Bit#	Buffer	Function
RB0/INT	bit 0	TTL/ST(1)	Input/output pin or external interrupt input. Internal software programmable weak pull-up.
RB1	bit 1	TTL	Input/output pin. Internal software programmable weak pull-up.
RB2	bit 2	TTL	Input/output pin. Internal software programmable weak pull-up.
RB3/PGM(3)	bit 3	TTL	Input/output pin or programming pin in LVP mode. Internal software programmable weak pull-up.
RB4	bit 4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5	bit 5	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB6/PGC	bit 6	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	bit 7	TTL/ST(2)	Input/output pin (with interrupt-on-change) or in-circuit debugger pin. Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode or in-circuit debugger.

3: Low-Voltage ICSP Programming (LVP) is enabled by default which disables the RB3 I/O function. LVP must be disabled to enable RB3 as an I/O pin and allow maximum compatibility to the other 28-pin and 40-pin mid-range devices.

Figure 3(a)

(b) Among these THREE (3) instructions, `RETURN`, `RETLW` and `RETFIE`, which one is the best instruction to use for returning from Interrupt Service Routine? Why?

(5 marks)

(c) The block diagram of the PIC16F877A analogue to digital converter (ADC) is shown in Figure 3(c)(i). The ADCON0 and ADCON1 registers are shown in Figure 3(c)(ii) and Figure 3(c)(iii) respectively. In this design, an internal voltage reference is selected, input channel 3 is selected, and the ADC is switched on but not running. Assume that channel 0, channel 1, channel 2 and channel 4 are configured as analogue input only. Also, assume that the conversion clock used is Fosc/8 with right justification on the result.

(i) What is the setting of the ADCON0 register?

(2 marks)

(ii) What is the setting of the ADCON1 register?

(2 marks)

(iii) Give one advantage of using an internal voltage reference or an external voltage reference.

(4 marks)

A/D Block Diagram

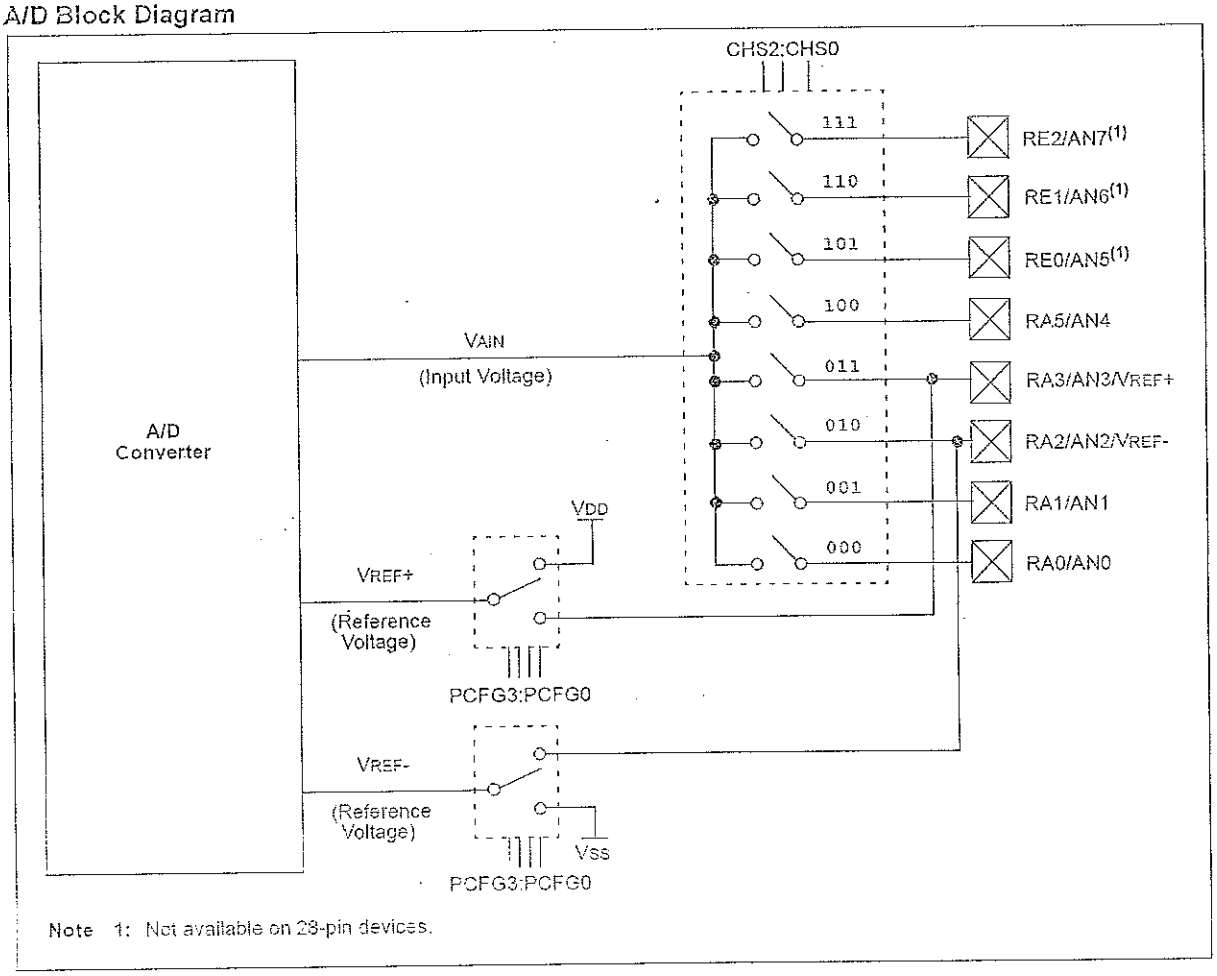

Figure 3(c)(i)

ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	—	ADON
bit 7							bit 0

bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits (ADCON0 bits in **bold**)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-3 **CHS2:CHS0:** Analog Channel Select bits

000 = Channel 0 (AN0)
001 = Channel 1 (AN1)
010 = Channel 2 (AN2)
011 = Channel 3 (AN3)
100 = Channel 4 (AN4)
101 = Channel 5 (AN5)
110 = Channel 6 (AN6)
111 = Channel 7 (AN7)

Note: The PIC16F873A/876A devices only implement A/D channels 0 through 4; the unimplemented selections are reserved. Do not select any unimplemented channels with these devices.

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion which is automatically cleared by hardware when the A/D conversion is complete)
0 = A/D conversion not in progress

bit 1 **Unimplemented:** Read as '0'

bit 0 **ADON:** A/D On bit

1 = A/D converter module is powered up
0 = A/D converter module is shut-off and consumes no operating current

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Figure 3(c)(ii)

ADCON1: A/D CONTROL REGISTER 1

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	ADCS2	—	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified. Six (6) Most Significant bits of ADRESH are read as '0'.

0 = Left justified. Six (6) Least Significant bits of ADRESL are read as '0'.

bit 6 **ADCS2:** A/D Conversion Clock Select bit (ADCON1 bits in shaded area and in bold)

ADCON1 <ADCS2>	ADCON0 <ADCS1:ADCS0>	Clock Conversion
0	00	Fosc/2
0	01	Fosc/8
0	10	Fosc/32
0	11	FRC (clock derived from the internal A/D RC oscillator)
1	00	Fosc/4
1	01	Fosc/16
1	10	Fosc/64
1	11	FRC (clock derived from the internal A/D RC oscillator)

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits

PCFG <3:0>	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0	VREF+	VREF-	C/R
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	AN3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	AN3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	AN3	VSS	2/1
011x	D	D	D	D	D	D	D	D	—	—	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	AN3	AN2	6/2
1001	D	D	A	A	A	A	A	A	VDD	VSS	6/0
1010	D	D	A	A	VREF+	A	A	A	AN3	VSS	5/1
1011	D	D	A	A	VREF+	VREF-	A	A	AN3	AN2	4/2
1100	D	D	D	A	VREF+	VREF-	A	A	AN3	AN2	3/2
1101	D	D	D	D	VREF+	VREF-	A	A	AN3	AN2	2/2
1110	D	D	D	D	D	D	D	A	VDD	VSS	1/0
1111	D	D	D	D	VREF+	VREF-	D	A	AN3	AN2	1/2

A = Analog input D = Digital I/O

C/R = # of analog input channels/# of A/D voltage references

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Note: On any device Reset, the port pins that are multiplexed with analog functions (ANx) are forced to be an analog input.

Figure 3(c)(iii)

(d) Describe the operation of the following assembly code snippet, and explain what the program accomplishes.

(5 marks)

```
COUNT   equ     h'40'
        movlw   .16
        movwf   COUNT
        bsf     5,7
 LOOP:  decf    COUNT, f
        btfss   3,2
        goto    LOOP
        bcf     5,7
NEXT    ---     -----
```

Question 4

(a) A Timer 2 block diagram is shown in Figure 4(a). Timer 2 is used to generate a delay of 50μs.

(i) Determine the value of the PR2 if the TMR2 is 0, the prescaler and postscaler of 1:1 are selected. Assume that the crystal clock is running at the frequency of 20MHz. Ignore the overhead due to instructions in the calculation.

(6 marks)

(ii) Explain how the microcontroller knows the delay of 50μs has reached.

(4 marks)

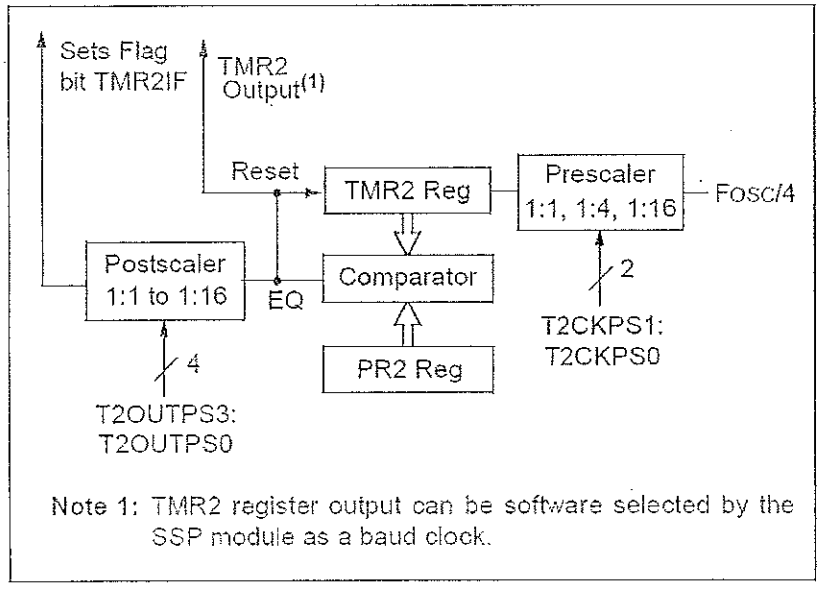

Figure 4(a)

(b) Provide the equivalent alternative instruction(s) that will perform the same outcome for each of the following instructions:

(i)
```
COMF   50H
COMF   51H
MOVF   50H, W
IORWF  51H, F
COMF   51H
```

(ii)
```
MOVLW  78H
ADDLW  88H
MOVWF  50H
```

(iii)
```
MOVF   50H, W
ADDWF  50H, F
```

(iv)
```
MOVF   30H, W
XORWF  30H, W
MOVWF  30H
```

(8 marks)

(c) Figure 4(c) shows the PIC to PIC communication via UART. Briefly explain the UART communication between these 2 PIC microcontrollers. Comment on the typical baud rate used for this communication. Assume the communication protocol used is 8N1. The figure below shows communication between two PIC16F877A microcontrollers.

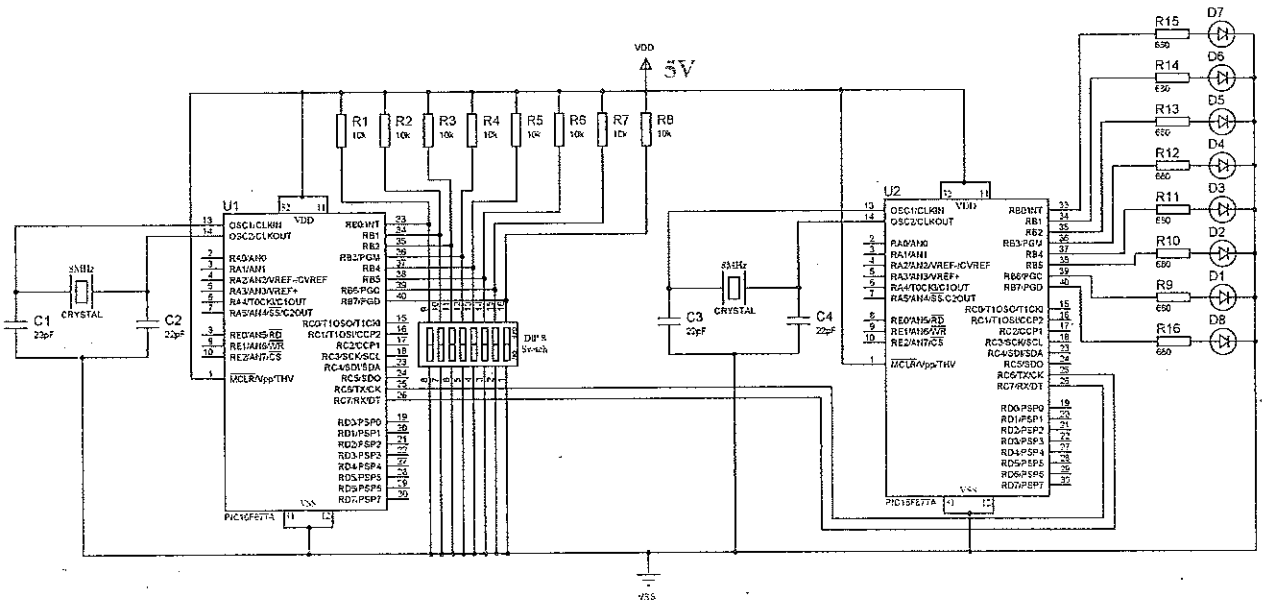

Figure 4(c)

(7 marks)

Question 5

(a) Calculate the time delay taken for Program 5(a) running at 4-MHz oscillator by the PIC16F628A microcontroller. Short all workings clearly for each instruction.

(7 marks)

Program

```
DELAY:
        MOVLW   0x36
DLOOP:  ADDLW   -1
        BTFSS   STATUS,2
        GOTO    DLOOP
        RETURN
```

Program 5(a) Coding

(b) Refer to Figure 5(b), the LCD requires THREE (3) "Control" lines from the microcontroller, namely Enable (E), Read/Write (R/W) and Register select (RS). Describe the function of each of the line.

(6 marks)

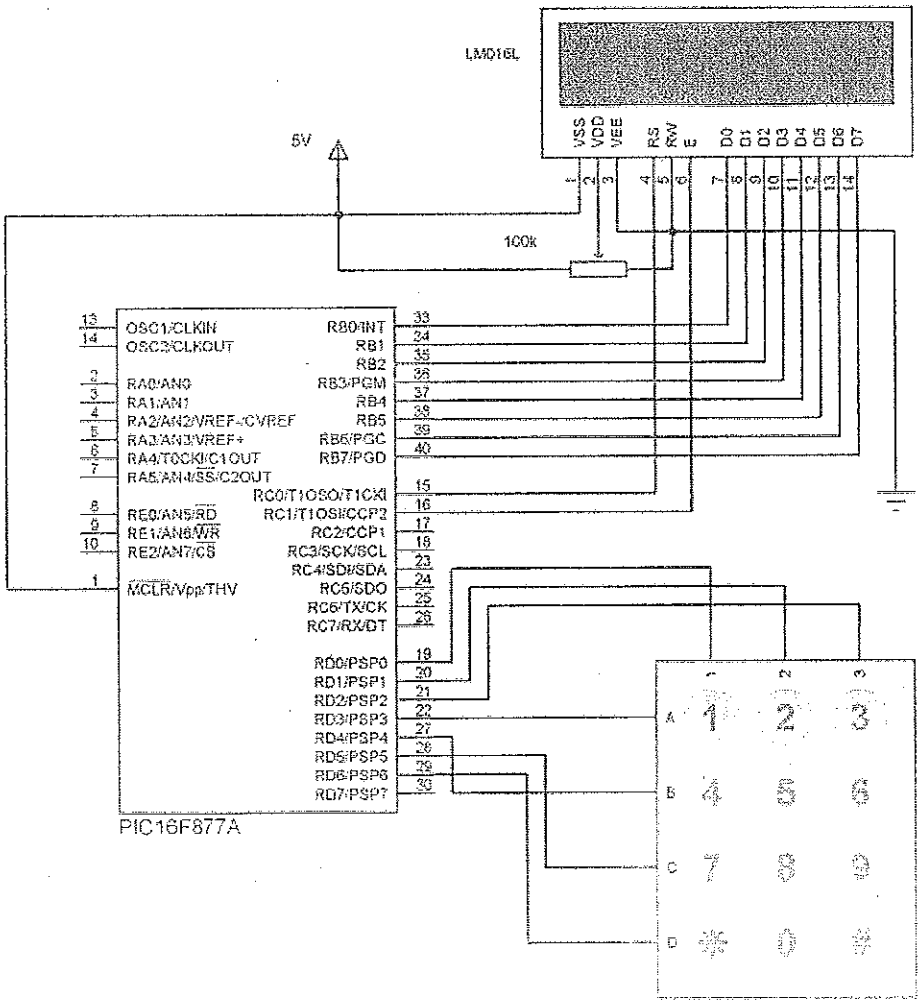

Figure 5(b)

(c) When the LCD display is not enabled, data lines are tri-state, what is meant by tri-state?
(3 marks)

(d) Using the LED008 Alphanumeric LCD Display (16 × 2) datasheet provided in Appendix D, clearly differentiate between CGROM, CGRAM and DDRAM with the aid of appropriate diagrams.
(9 marks)

Question 6

(a) Embedded software is directly linked to the electronic hardware.

(i) Complete Table 6(a) truth table.
(3 marks)

(ii) Draw a schematic diagram showing the interface between PIC16F877A microcontroller and a common cathode 7-segment display.
(6 marks)

(iii) Write an assembly program to output the display letters continuously (PLC16F874A) one at a time, in sequence of P to A as shown in Figure 6(a)(ii). Also, include comments for any instruction used.
[Refer to Appendix for Instruction Set]
(12 marks)

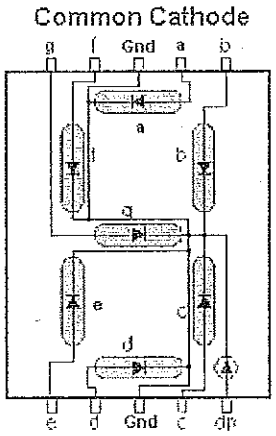

Figure 6(a)(i)

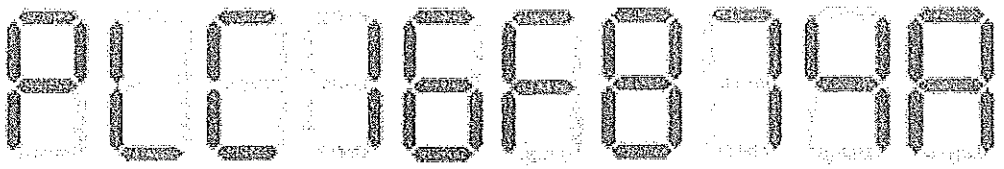

Figure 6(a)(ii)

dp	g	f	e	d	c	b	a	Hexa	Display
0	1	1	1	0	0	1	1	73H	P
0	.	.	.	.	.	.	.	.	L
0	.	.	.	.	.	.	.	.	c
0	.	.	.	.	.	.	.	.	1
0	.	.	.	.	.	.	.	.	6
0	.	.	.	.	.	.	.	.	F
0	.	.	.	.	.	.	.	.	8
0	.	.	.	.	.	.	.	.	7
0	.	.	.	.	.	.	.	.	4
0	1	1	1	0	1	1	1	77H	A

Table 6(a)

(b) What is the main difference between an assembler directive and an assembly instruction? (4 marks)

– THE END –

EEE2114(F)/Aug16/Steven Khoo/15/09/16