INTI International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2016**
Programme	:	Diploma in Electrical and Electronic Engineering
Course	:	**EEE2105: Introduction To Microprocessors**
Date of Examination	:	5 December 2016 (Monday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Appendix A (8086 Instruction Set Summary), Appendix B (ASCII Table), Appendix C (8255 PPI), Appendix D (8253/8254 PIT), Appendix E (8259 PIC)

Examiner(s) : **Mr. Steven Khoo Boo Tap**

Moderator : Dr. Mandeep Singh

This paper consists of 12 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2105: INTRODUCTION TO MICROPROCESSORS
FINAL EXAMINATION: AUG2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Calculate the address range for Y1, Y4 and Y7 of the 74LS138 active-low decoder for the following design.

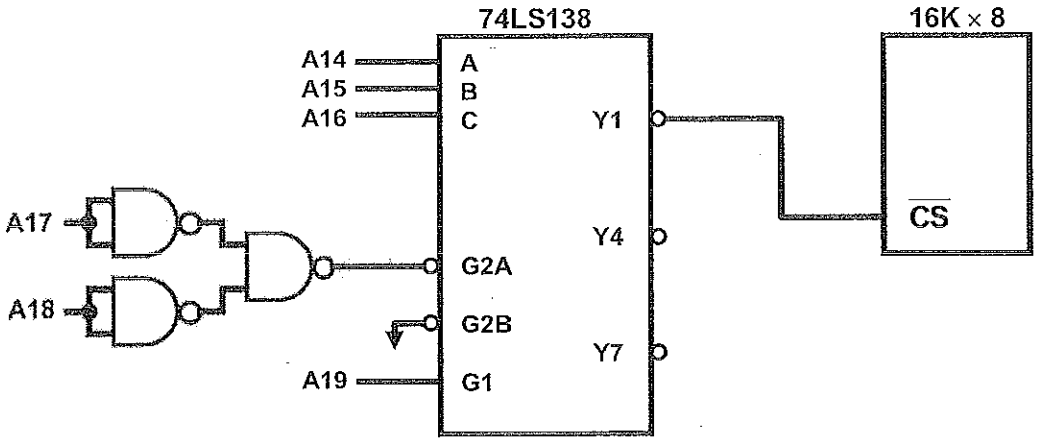


Figure 1(a)

(7 marks)

(b) Comment on the validity of the following instructions. Explain why if it is not valid. Provide the addressing mode if the instruction is valid.

(i) MOV CX, [AX]

(2 marks)

(ii) MOV AL, [BP][BX][DI][SI] 33H

(2 marks)

(iii) MOV CS, DS

(2 marks)

(iv) MOV BL, [BX+0BH]

(2 marks)

(c) Perform the following number system transformation. Show all workings clearly.

(i) $A4.F4_{16}$ to decimal equivalent with 6 decimal points accuracy. (2 marks)

(ii) $[10215.01_8 \times 12_8]$ to hexadecimal equivalent with 2 hexadecimal points accuracy. (4 marks)

(iii) $[164.953125_{10} - 11.101_{16}]$ to binary equivalent with 12 binary points accuracy. (4 marks)

Question 2

(a) Explain the term of the following with an appropriate diagram.

(i) Simplex (3 marks)

(ii) Half-Duplex (3 marks)

(iii) Full-Duplex (3 marks)

(b) At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal)

Registers

	H	L
AX	2C	10
BX	00	04
CX	10	01
DX	2B	33
CS	02	00
DS	90	00
SS	40	10
ES	61	00
BP	00	1F
SP	00	05
IP	11	0B
SI	21	34
DI	FF	FF

Memory

9000B	12
9000A	34
90009	56
90008	78
90007	9A
90006	BA
90005	DE
90004	F0
90003	21
90002	43
90001	09
90000	67
8FFFF	54
8FFFE	DF

4010E	6F
4010D	2D
4010C	C1
4010B	25
4010A	3F
40109	12
40108	FF
40107	FC
40106	E1
40105	10
40104	00
40103	36
40102	21
40101	88

(i) What is the physical address of the next instruction to be executed?

(2 marks)

(ii) What is the physical address of the top of the stack?

(2 marks)

(iii) Draw a memory map for the 8086 microprocessor, indicating clearly the start and end addresses of the segments.

(3 marks)

(iv) Provide the registers and memory locations that are effected, and their new values after the execution of SUB [BX + 06H], AX.

(3 marks)

(c) What is the different between JMP (Unconditional Jump) and CALL (Unconditional Call) instructions? Provide FOUR (4) detail comparisons.

Illustrate clearly using an appropriate example to show the differences. Use same data for the comparison of both the instruction.

(6 marks)

Question 3

(a) A 10-MHz 8086 based system is using ROM of 650-ns speed. Calculate the number of wait states that the ROM selection circuitry must add if the delay due to data path and decoding circuitry (74LS138, and so on) is 45-ns.

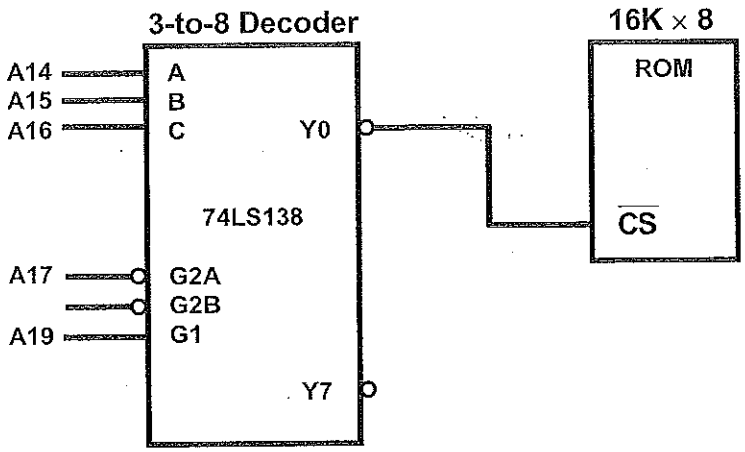


Figure 3(a) 8086 Based System

(5 marks)

(b) The 8255 PPI is configured as shown in Figure 3(b). Write a program to count the number of 'zeroes" in the incoming data received from port C continuously via 8255 PPI. The result will be sent to port A if the count result is even and sent to port B if the count result is odd. Assume the configuration below is using Mode 0.

Also, include comments for any instruction used. The program length should be as minimum as possible.

(12 marks)

Examples of incoming data and the respective action:

- 25_H (**00100101**) ⇨ send 05_H (Odd) out to port B
- CC_H (**11001100**) ⇨ send 04_H (Even) out to port A
- 00_H (**00000000**) ⇨ send 08_H (Even) out to port A
- EF_H (**11101111**) ⇨ send 01_H (Odd) out to port B
- FF_H (**11111111**) ⇨ send 00_H (Even) out to port A
- 73_H (**01110011**) ⇨ send 03_H (Odd) out to port B

[Refer to Appendix C for 8255 PPI Control Word]

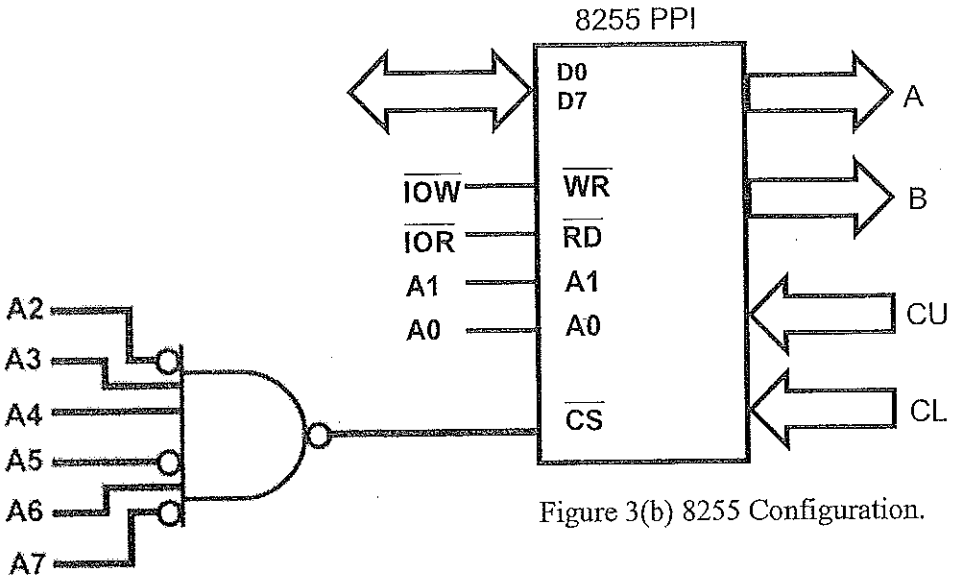


Figure 3(b) 8255 Configuration.

(c) Describe the function of the following pins of 8086 microprocessors.

(i) RESET [pin 21]

(2 marks)

(ii) READY [pin 22]

(2 marks)

(iii) NMI [pin 17]

(2 marks)

(iv) INTR [pin 18]

(2 marks)

Question 4

(a) Given the registers and the memory locations contents of 8086 as follows: (All values are in Hexadecimal).

Registers					
AX	1234H	CS	3010H	DI	0555H
BX	0404H	DS	5F41H	SI	5060H
CX	5678H	SS	5F81H	BP	6070H
DX	789AH	ES	7040H	IP	7100H

Table 4(a-1) Registers and the content

Memory																
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
5F800H	11	22	33	44	55	66	77	88	99	00	A1	B1	C1	D1	E1	F1
5F810H	02	04	45	78	90	11	22	33	44	55	66	77	88	99	00	12
5F820H	34	56	78	90	12	34	56	78	90	12	34	56	78	90	11	22
5F830H	33	44	55	66	77	88	99	00	10	A0	12	34	56	78	9A	BC
5F840H	DE	F0	00	11	00	11	10	21	99	B8	77	33	58	45	33	22
5F850H	25	31	19	00	01	22	20	31	89	C8	66	22	CC	54	44	06
5F860H	DC	F0	20	18	02	33	30	41	79	D8	55	11	BB	67	55	20
5F870H	FE	F1	10	12	03	44	40	51	69	E8	44	AA	55	76	66	21
5F880H	00	FF	00	FF	00	FF	00	60	5F	FF	14	00	FF	F1	80	09

Table 4(a-2) Memory locations and the content

Perform the following operations. Indicate the result in the register and the content where it is stored. The operations are independent of each other. Show all workings of before and after with appropriate diagram illustration.

(i) SUB [0416H – 22], DX

(3 marks)

(ii) AND [BP] + 23 + 23H – 60213o, BH

(3 marks)

(iii) OR [DI] + 101b + 101o – 101 – 101H, AX

(3 marks)

(iv) XOR [SI + BP + 0EB0H – BFADH + 10010000b], CX

(3 marks)

(b) Calculate the time delay taken for Program 4(b) running on 8086 microprocessor at 10-MHz. At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal).

Assume that DS register contains 0700H. Show all workings clearly for each instruction.

(13 marks)

[Refer to Appendix A for the cycle time]

Memory																
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
07700H	08	04	45	78	10	21	22	33	34	25	26	27	28	49	40	14
07800H	02	03	05	01	12	24	56	01	10	00	34	56	98	50	19	62
07900H	07	20	30	40	50	60	70	80	90	03	00	C0	D0	E0	F0	00
07A00H	1D	1C	1B	1A	19	18	55	66	47	46	02	44	43	42	41	0F
07B00H	18	19	23	48	25	26	27	58	29	31	32	35	36	37	38	39

Table 4(b) Random Address Memory

Program		
	MOV	AL, 02H
LOOP4:	MOV	BL, [0A0AH]
LOOP3:	MOV	DX, [0808H]
LOOP2:	MOV	CX, [0909H]
LOOP1:	NOP	
	NOP	
	LOOP	LOOP1
	DEC	DL
	JNZ	LOOP2
	NOP	
	DEC	BL
	JNZ	LOOP3
	XOR	AL, AL
	JNZ	LOOP4
	HLT	

Program 4(b) Coding.

Question 5

(a) A 10-MHz 8086 microprocessor is interfacing with a 3-MHz 8237 DMA. The CPU bus cycle uses two wait states and the bus cycle for the DMA is 4 clocks. Calculate the DMA data transfer rate if the system bus is used alternately by the CPU and DMA. Express the answer in Kbytes/s.

(6 marks)

(b) A transmission system uses three asynchronous serial data communication settings to transmit a passcode that contain 9 characters to the receiver via 8250 UART chip.

Figure 5(b-1) is used to transmit the first 3 characters, followed by Figure 5(b-2) setting for the next 4 characters and finally, Figure 5(b-3) setting for the last 2 characters of the transmission.

The **LSB** is transmitted first.

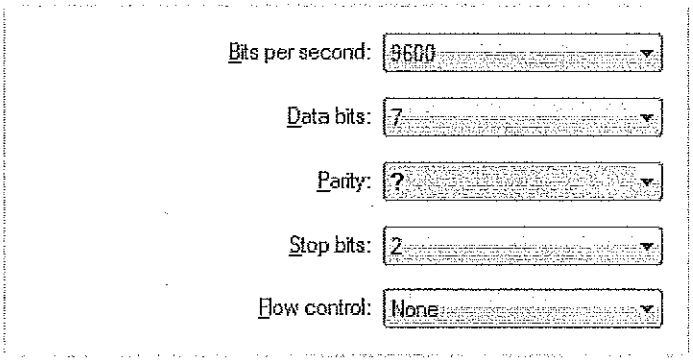


Figure 5(b-1) First 3 characters setting.

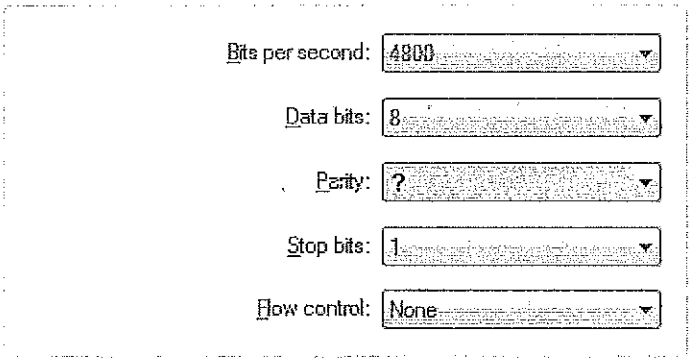


Figure 5(b-2) Next 4 characters setting.

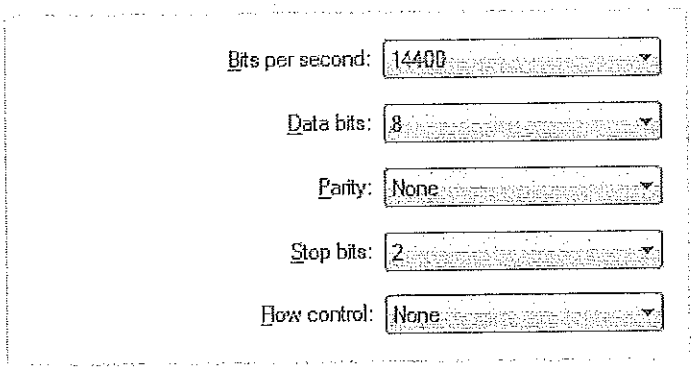


Figure 5(b-3) Last 2 characters setting.

Decode the following serial data received in continuous ASCII characters message:

Incoming data:

01110110111001011111110101101001100001110001010111100010100111001100101111001001101111111011001100110011

(i) What is the passcode transmitted and passcode solution?

(10 marks)

(ii) What is the Parity setting used for Figure 5(b-1) and Figure 5(b-2)?

(2 marks)

(iii) Calculate the total time when transmitting the above message and the time wasted due to overhead.

(3 marks)

[Refer to Appendix B for ASCII codes]

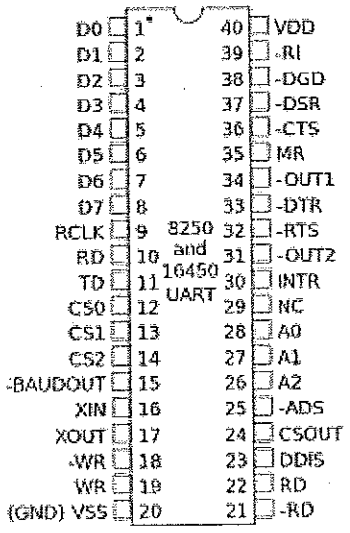


Figure 5(b-4) 8250 UART pin configuration.

(c) The 8259 PIC is configured as shown in Figure 5(c). Write a program to initialize the 8259 using the port addresses in Figure 5(c). Assume the ICW1 is 1BH, ICW2 is 58H, no ICW3 and ICW4 is 2FH. Also include comments for any instruction used.

(4 marks)

[Refer to Appendix E for 8259 PIC Control Words]

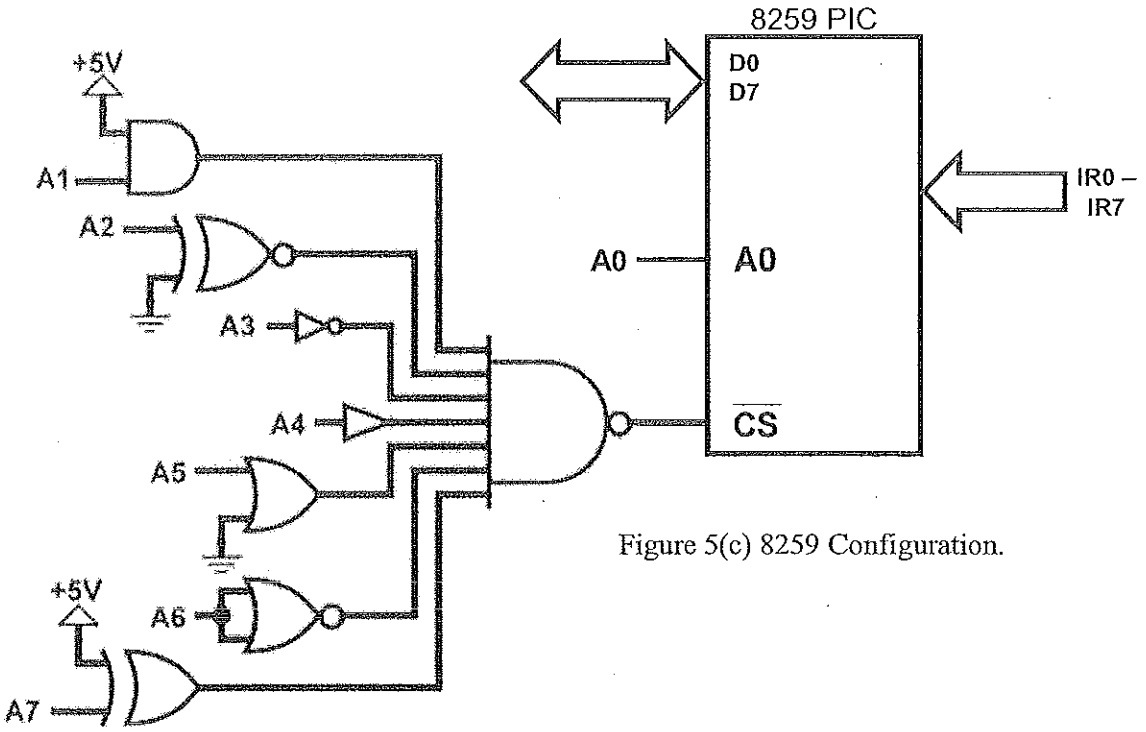


Figure 5(c) 8259 Configuration.

Question 6

(a) Figure 6(a-1) shows a TM4100GAD8 Dynamic RAM Module pin configuration.
Figure 6(a-2) shows a TM124MBK36E Dynamic RAM Module pin configuration.

Determine the following:

(i) total memory capacity of the area (A and B) memory device in Kbits,

(4 marks)

(ii) individual memory organization,

(2 marks)

(iii) number of address pins and number of data pins of each memory device.

(4 marks)

Figure 6(a-2) TM124MBK36E DRAM Module pin configuration.

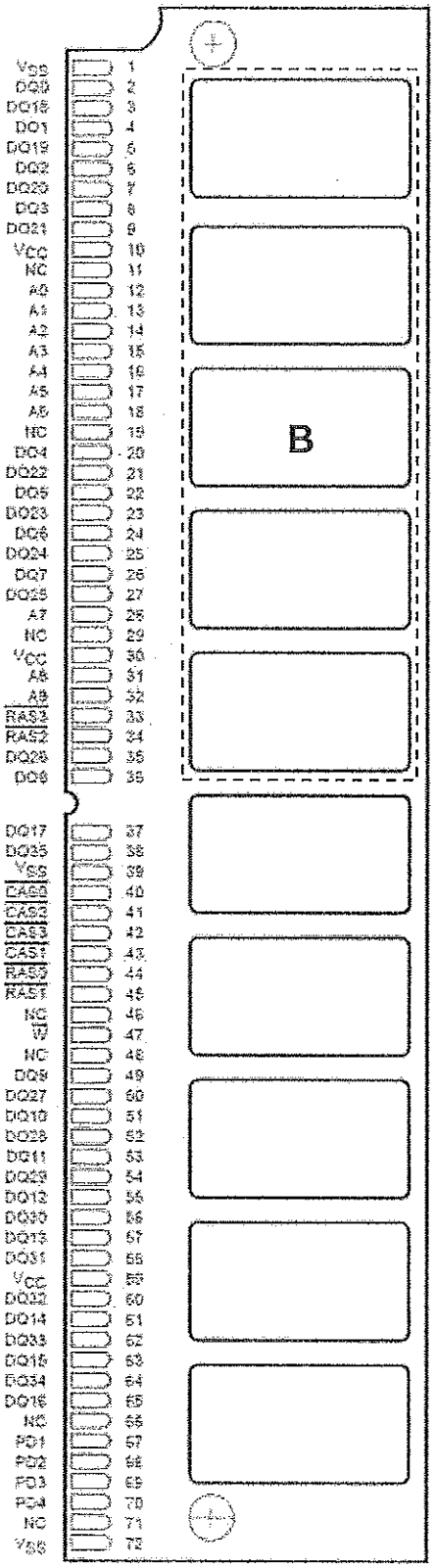
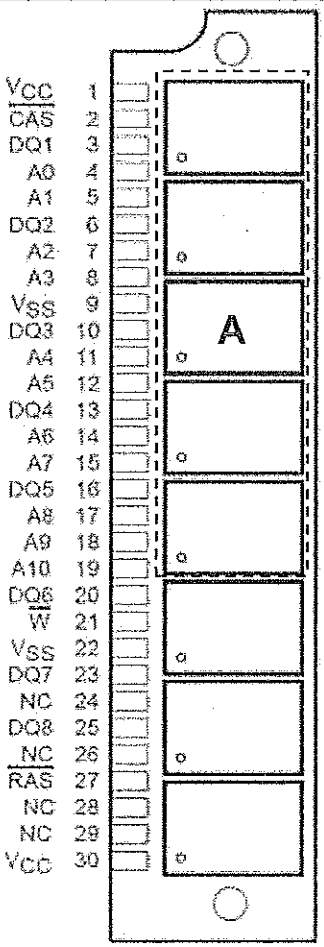


Figure 6(a-1) TM4100GAD8 DRAM Module pin configuration.



(b) With the aid of a suitable diagram with details labelling, illustrate step-by-step how DMA can be used to speed up CPU operation during the transfer of data from memory to an I/O device.

The diagram should include the control signals for Microprocessor (CPU), DMA, Memory and I/O Device. The steps describe should be as detail as possible describing all control signals operation.

(10 marks)

(c) The 8254 PIT chip is configured as shown in Figure 6(c). CLK1 of counter 1 is 1.19318-MHz and Gate1 is connected to high permanently. Counter 1 generates a periodic pulse every 45.2573-μs to refresh DRAM memory of the computer. Write assembly instructions to generate this periodic pulse through OUT1.

(5 marks)

[Refer to Appendix D for 8253/8254 PIT Control Word]

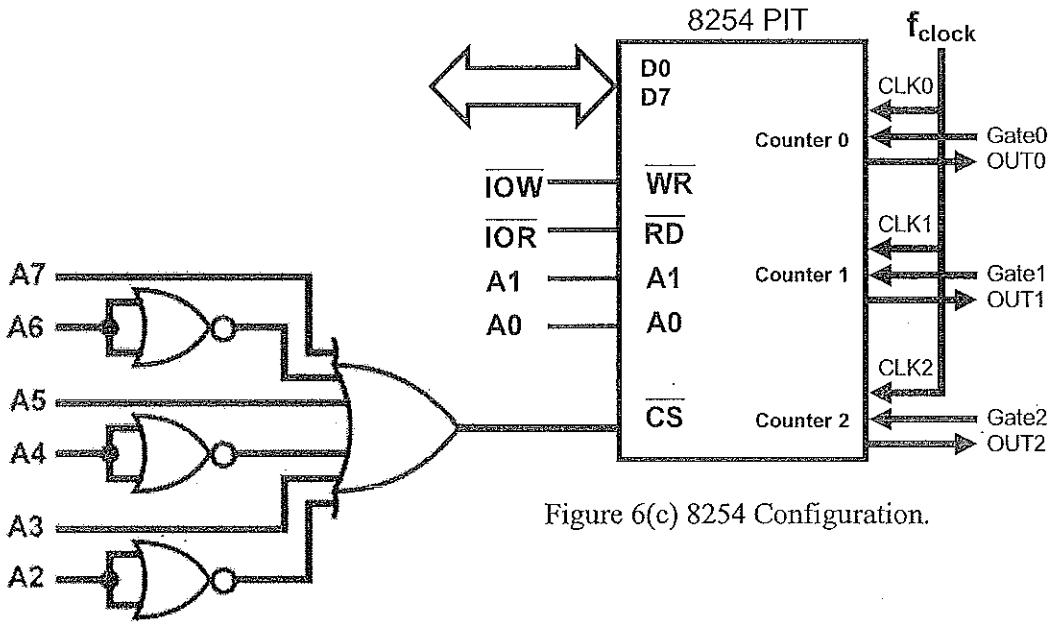


Figure 6(c) 8254 Configuration.

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EEE2105(F)/Aug16/Steven Khoo/17/08/16