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FINAL
Examination Paper

(COVER PAGE)

Session : AUGUST 2016

Programmes : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE2102: INTRODUCTION TO POWER ELECTRONICS

Date of Examination : 8 December 2016 (Thursday)

Time : 8:00am – 10:00aim

Duration : 2 Hours Reading Time : Nil

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.

Materials Permitted : Scientific Calculator (Model fx570 Series)

Materials Provided : Worksheet-Q1 and Worksheet-Q5
Graph Paper
Laplace Transformation Table

Examiner(s) : Chan Tse Wei

Moderator : Dr. Ooi Beng Lee

This paper consists of 8 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2102: INTRODUCTION TO POWER ELECTRONICS
FINAL EXAMINATIONS: AUGUST 2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

a. i. Explain the reason power electronics is primarily based on high frequency switching scheme to control and convert electric power delivered to a load. [4]

ii. State four application areas of power electronics. [4]

iii. State four power electronic components. [4]

b. Figure-Q1(b) shows the voltage and current timing diagrams for a power device.

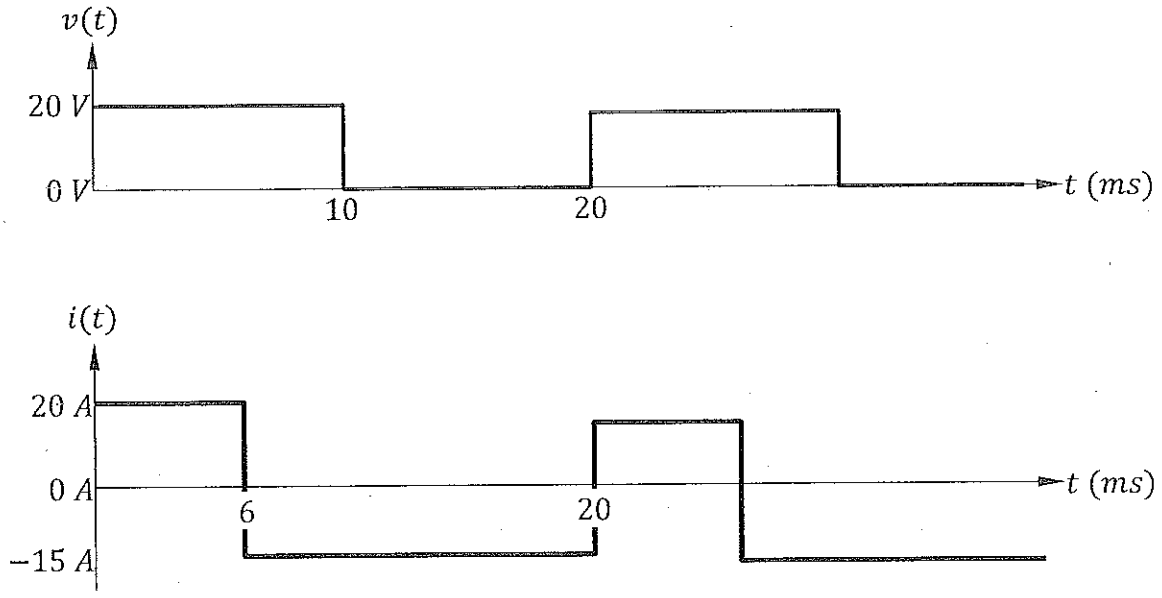


Figure-Q1(b)

i. Sketch the timing diagram of the power delivered to the load in "Worksheet-Q1". [3]

ii. Determine the duration within the first period where the device is switched on. [2]

iii. Determine the energy delivered to the device in one period. [4]

iv. Determine the average power delivered to the device in one period. [4]

Question 2

a. State the function of a rectifier and explain the differences between a controlled rectifier and an uncontrolled rectifier. [6]

b. Figure-Q2(b) shows power electronic circuit in which switch S models an ideal switching device, which closes at $t = 0\ s$, and the initial voltage of the capacitor C, $v_o(0) = 0\ V$ and the initial current $i(0) = 0\ A$. Diode D is assumed ideal.

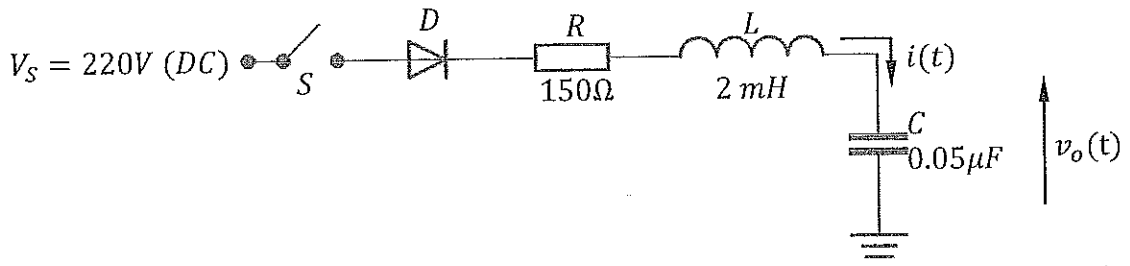


Figure-Q2(b)

i. Derive the current expression of $i(t)$ when switch S is turned on at $t = 0\ s$. [6]

ii. Determine the conduction time of the diode. [4]

iii. Plot $i(t)$ for the first 50 μs on the graph paper provided. [9]

Question 3

a. i. State one advantage and one disadvantage of power transistors as compared to thyristors in power electronic applications. [4]

ii. Explain the requirement(s) to drive a bipolar junction transistor (BJT) into saturation, and state the characteristic of a saturated BJT. [4]

iii. Draw the large signal DC operation model of a power NPN transistor which includes a current dependent current source, the junction diodes and the collector leakage current. [4]

b. Figure-Q3(b) shows a BJT switching circuit. The transistor is characterized as follows:

β = varies from 12 to 75

$V_{CE_{sat}} = 1.2\ V$

$V_{BE_{sat}} = 1.6\ V$

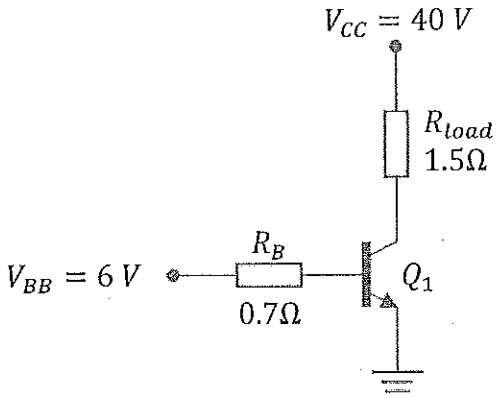


Figure-Q3(b)

Determine,

i. the overdrive factor, ODF [3]

ii. the forced factor, β_f [3]

iii. the power loss in the transistor, P_T [3]

iv. the power efficiency of the circuit. [4]

Question 4

a. State four advantages and two disadvantages of power MOSFET over power BJT. [6]

b. Sketch and clearly label a linearized transfer curve (i_D vs v_{GS}) of an enhancement type n-channel power MOSFET. [3]

c. Draw the steady-state model of an enhancement type n-channel power MOSFET and define all the parameters used in the model. [6]

d. Figure-Q4(d)(i) shows a simple MOSFET based switching circuit. The wave shape of V_G is show in Figure-Q4(d)(ii).

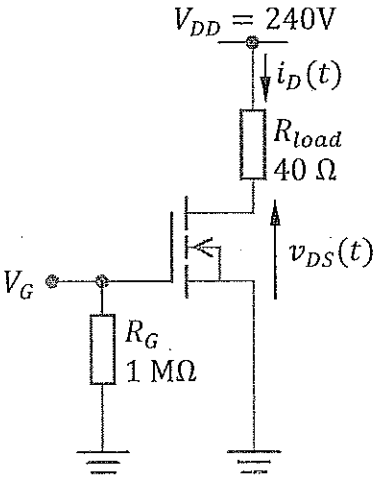
The MOSFET has the following specifications:

Drain current rise time, $t_r = 2\mu s$

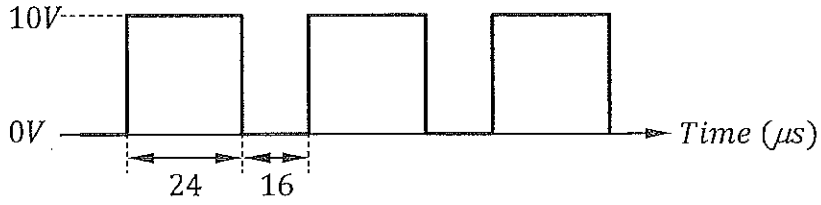
Drain current fall time, $t_f = 3\ \mu s$

$R_{DS(ON)} = 5\Omega$

Drain-source leakage current, $I_{DSS} = 3\ mA$



(i) MOSFET switching circuit.



(ii) Wave shape of V_G.

Figure-Q4(d)

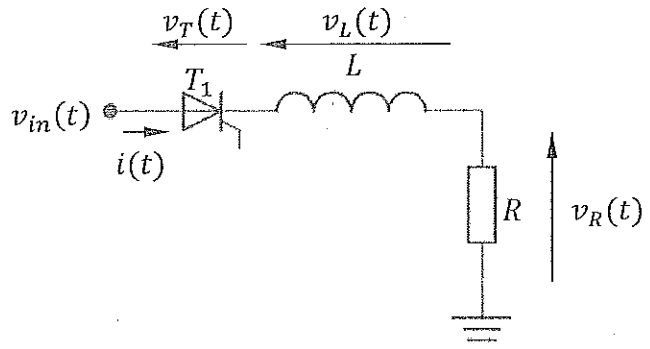
i. Calculate the steady-state load current, $I_{D(max)}$ during ON state. [2]

ii. Calculate the saturated voltage across the drain and source terminals, $V_{DS(sat)}$. [2]

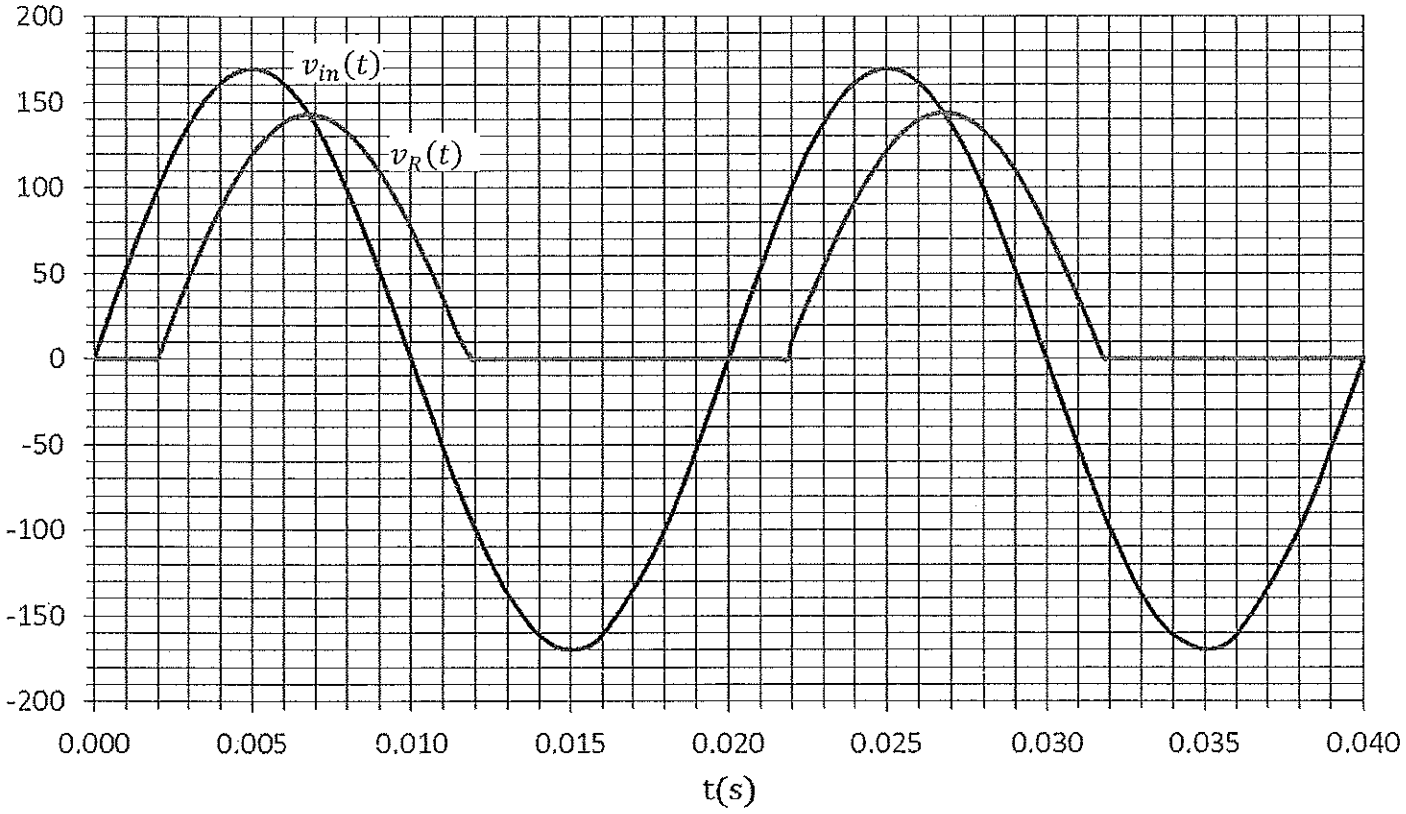
iii. Assume piecewise linear operation, sketch the respective timing diagram for $i_D(t)$ and $v_{DS}(t)$, synchronized with the waveform of V_G. [6]

Question 5

Figure-Q5(i) shows a controlled half-wave rectifier circuit with RL load, while Figure-Q5(ii) shows the timing diagram of $v_{in}(t)$ and $v_R(t)$ respectively.



(i)



(ii)

Figure-Q5

a. Approximate the firing angle, α, of thyristor T_1. [3]

b. Approximate the extinction angle, β, of thyristor T_1. [3]

c. Based on the answers obtained in part (a) and (b), determine the conduction angle, γ, of thyristor T_1. [2]

d. Sketch the timing diagrams as accurate as possible for $v_L(t)$ and $v_T(t)$ respectively, on the given "Worksheet-Q5". Assume ideal thyristor operation. [10]

e. For the circuit in Figure-Q5(i), the instantaneous current, $i(t)$, within $\alpha \leq \omega t \leq \beta$, is expressed as,

$$i(t) = \frac{V_m}{\sqrt{R^2 + \omega^2 L^2}}\left[\sin\left(\omega t - \tan^{-1}\left(\frac{\omega L}{R}\right)\right) - \sin\left(\alpha - tan^{-1}\left(\frac{\omega L}{R}\right)\right) e^{-\frac{R}{\omega L}(\omega t - \alpha)}\right]$$

Where,

V_m = amplitude of the input sinewave

α = firing angle of thyristor T_1 in radians

β = extinction angle of thyristor T_1 in radians

ω = input frequency in rad/s

Determine the average current, I_{DC} that flows through the circuit if $R = 20\ \Omega$ and $L = 0.04\ H$. [7]

Question 6

a. i. What is a DC chopper circuit? [2]

ii. What is the difference between buck chopper and boost chopper? [2]

iii. State one advantage of DC chopper circuits. [1]

b. Figure-Q6(b) shows a chopper circuit.

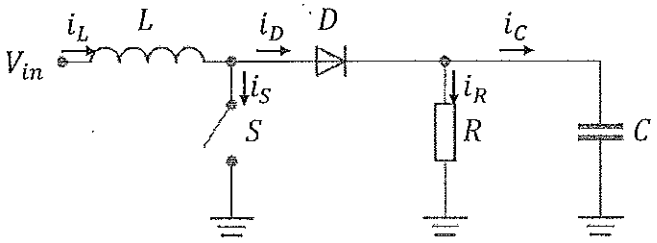


Figure-Q6(b)

i. Comment on the characteristic of the circuit in relation to the duty cycle, D. [4]

ii. Quantitatively show that the voltage across resistor R is given as,

$$V_R \approx \frac{V_{in}}{1-D}$$

where D is the duty cycle of the switching action. Show all workings clearly and state the assumption made. [8]

iii. For a specific value of D, derive an expression to calculate the minimum value of inductance, L in terms of R, D and the period of switching action, T where the input current is continuous. Assume power loss is negligible. [8]

~ The End ~