INTI International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2016**
Programme	:	Diploma in Electrical and Electronic Engineering
Course	:	**EEE2101: Introduction To Digital Electronics**
Date of Examination	:	6 December 2016 (Tuesday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Nil

Examiner(s) : **Mr. Steven Khoo Boo Tap**

Moderator : **Mr. Kevin Tan Geok Su**

This paper consists of 11 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: AUG2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the letter LnOPqrStUy, respectively, as shown below in Figure 1(a-1). The BCD inputs are labelled as WXYZ, W is the MSB and Z is the LSB. Figure 1(a-2) shows a Common-Cathode 7 segment display. Assume all unused inputs as don't care.

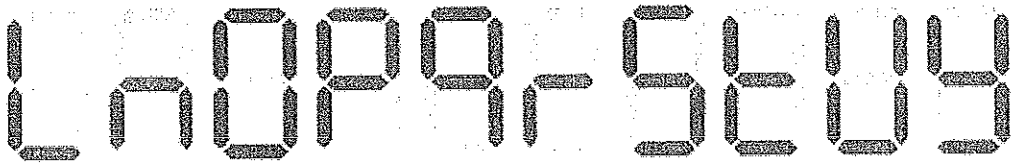


Figure 1(a-1)

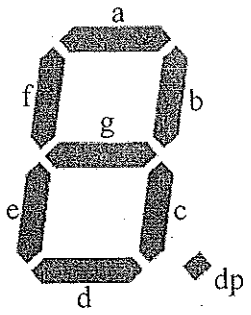


Figure 1(a-2)

(i) Develop the truth table for the inputs to segments a through g of the 7 segment. (4 marks)

(ii) Determine the SOP form of the logic expression for segments f and g. (6 marks)

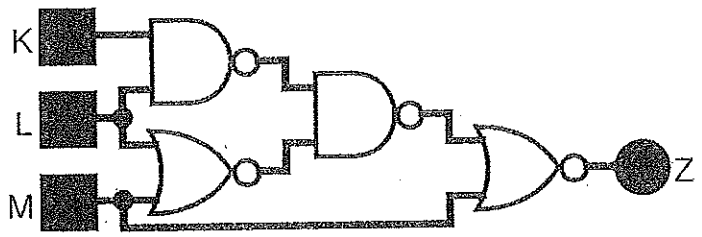
(iii) Implement the logic expression using only 3-input NAND gate with minimum 7410 ICs consideration. State the number of ICs used. Show all working clearly. (7 marks)

(b) Using Boolean algebra only, simplify to the simplest logic gate(s):

(i) $Y = \overline{AC} \cdot \overline{ABC \cdot \overline{B}} + \overline{A} \cdot \overline{B} \cdot \overline{C}$

(4 marks)

(ii)



(4 marks)

Question 2

(a) Design a synchronous 3-bit up/down Gray code counter using positive edge-triggered D flip-flops only. Assume D_A is the MSB and D_C is the LSB inputs. Input Y will be used as the up/down controller. The counter will count from 000 ⇨ 001 ⇨ 011 ⇨ 010 ⇨ 110 ⇨ 111 ⇨ 101 ⇨ 100 ⇨ 000 for counting up when input, Y = 0 and 000 ⇨ 100 ⇨ 101 ⇨ 111 ⇨ 110 ⇨ 010 ⇨ 011 ⇨ 001 ⇨ 000 for counting down when input, Y = 1. Use $Q_AQ_BQ_C$ outputs labelling for D_A, D_B and D_C inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.

(i) Provide the excitation table used and the state diagram.

(2 marks)

(ii) Provide the transition table/ next state table.

(4 marks)

(iii) Simplify using Karnaugh map and Boolean algebra if necessary.

(6 marks)

(iv) Draw the complete logic circuit diagram with proper label.

(5 marks)

(b) Implement $F(A,B,C) = \Sigma(0,3,4,5)$ using the following in the simplest form:

(i) SN7402N (2-input NOR gates) only.

(4 marks)

(ii) SN74157N (2-to-1 Multiplexer) with B as select line and other logic gate(s).

(4 marks)

Question 3

(a) Table 3(a) and Table 3(b) show a portion of a dual positive edge-triggered JK flip-flops (DM7476) and a triple 3-input AND gate datasheet respectively. Figure 3(a) show the logic circuit diagram of an asynchronous counter which uses positive edge-triggered JK flip-flops with labelling of $Q_AQ_BQ_CQ_D$ where Q_D is MSB and Q_A is LSB. Assume the environment is at $T_A = 25°C$ with $V_{CC} = 5V$.

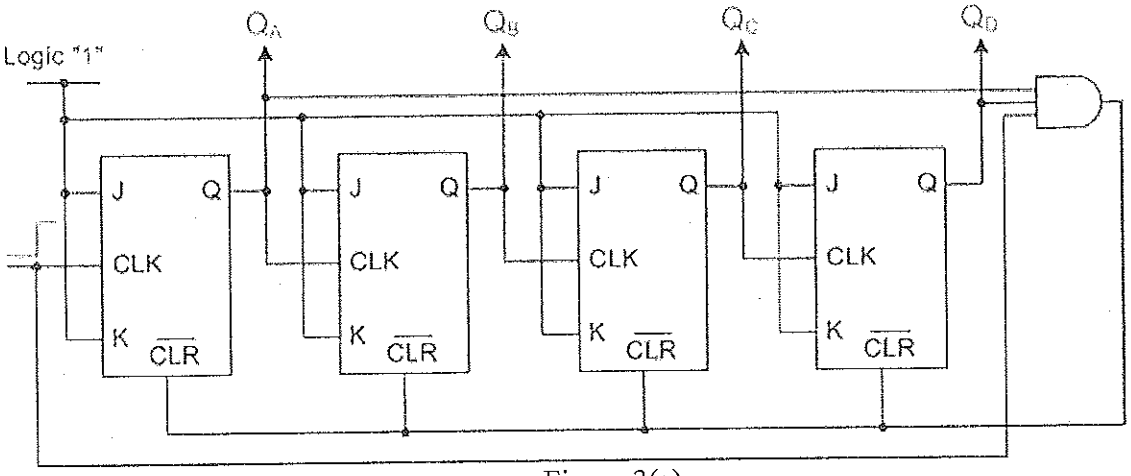


Figure 3(a)

Switching Characteristics
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		25	ns

Table 3(a) JK flip-flop

Symbol	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
t_{PLH}	A, B or C	Y	C_L = 15 pF, R_L = 2kΩ		8	27	ns
t_{PHL}					10	19	ns

Table 3(b) AND gate

(i) Determine the total propagation delay from the given datasheets in Table 3(a) and Table 3(b).

(5 marks)

(ii) Determine the maximum frequency at which the counter can be operated stably.

(3 marks)

(iii) Show the output timing diagram of Figure 3(a) and state the function of this counter.

(5 marks)

(b) Perform the following number system transformation. Show all workings clearly.

(i) $[3020.3020_8 - 1002.1002_8]$ to decimal equivalent with 6 decimal points accuracy.

(4 marks)

(ii) $[106.01_8 \times 1.6_8]$ to binary equivalent with 8 binary points accuracy.

(4 marks)

(iii) $[163.0703125_{10} - 11.101_8]$ to hexadecimal equivalent with 3 hexadecimal points accuracy.

(4 marks)

Question 4

(a) Assume that the numbering system used is a 12-bit system. Show all working clearly. Express the decimal number +2018 and –2018 in the sign-magnitude, 1's complement and 2's complement form as shown in the Table 4(a).

	+2018	–2018
Sign-magnitude		
1's complement		
2's complement		

Table 4(a)

(4 marks)

(b) Figure 4(b) below shows a 4-bit synchronous counter which is designed so that it performs a special counting sequence. Analyse its operation by determining its counting sequence. Assume that all flip-flops are initially in the 0 state (0000) for $Q_3Q_2Q_1Q_0$. Flip-flop FF3 is MSB and FF0 is LSB. Use J_3K_3, J_2K_2, J_1K_1 and J_0K_0 inputs labelling for Q_3, Q_2, Q_1 and Q_0 outputs. Show all workings clearly.

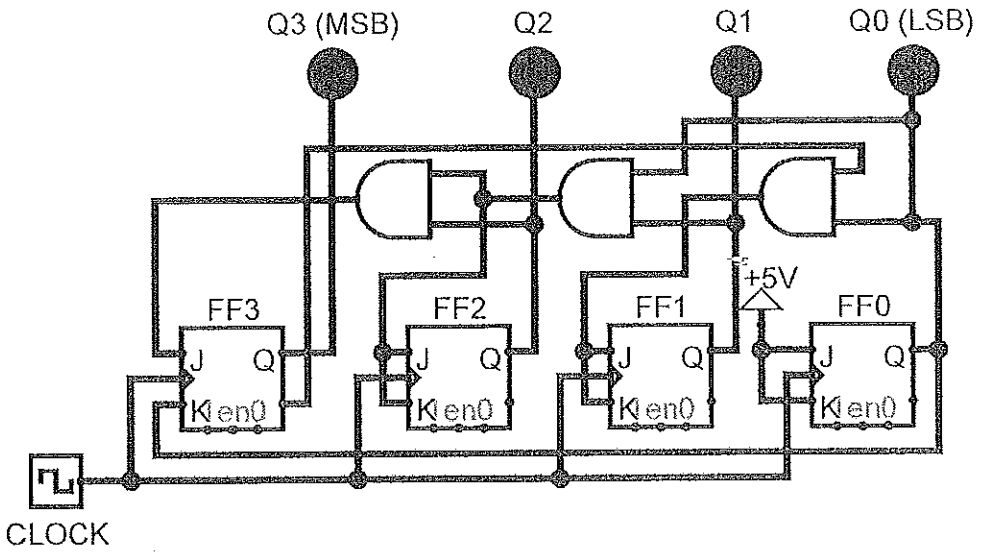


Figure 4(b)

(i) Provide the Boolean expressions from the logic circuit.

(2 marks)

(ii) Provide all Karnaugh maps according to the expressions.

(4 marks)

(iii) Provide the transition table/ next state table with excitation table.

(5 marks)

(iv) Draw the state diagram and comment on the outcome of the states obtained.

(4 marks)

(c) A binary-weighted-input DAC is shown in Figure 4(c). If the LSB bit resistor has a value of 240kΩ, compute the values of the other input resistors. Also, calculate the V_{out} if the DAC has a binary input of 1011 with Logic 1 (HIGH) as +4.0V and Logic 0 (LOW) as 0V. Assume that R_f equals to 15kΩ. What are the disadvantages of this method of DAC?

(6 marks)

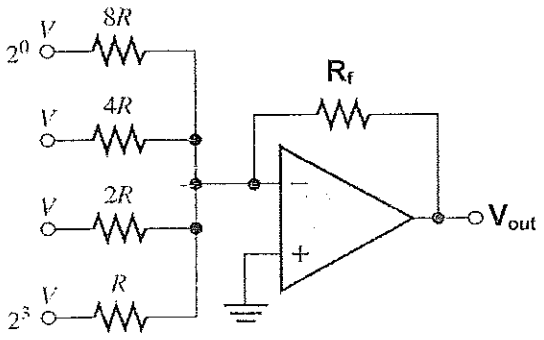
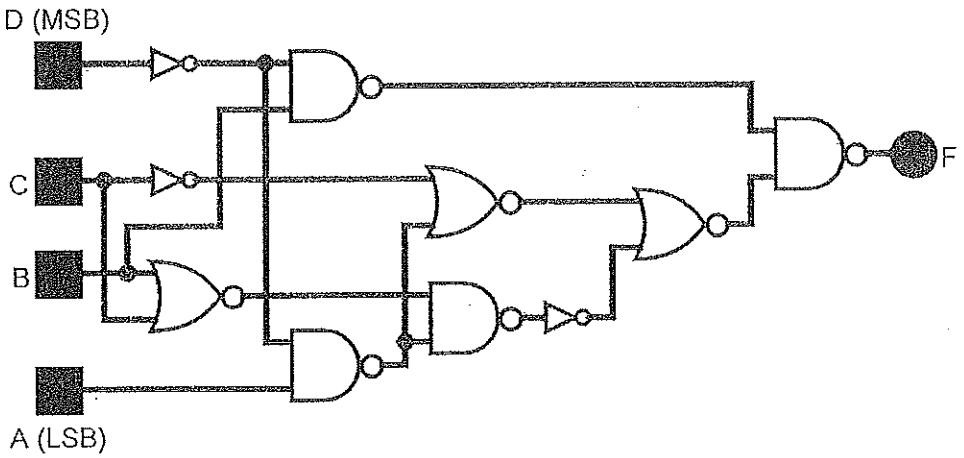


Figure 4(c)

Question 5

(a) Use the given Karnaugh map and/or Boolean algebra to obtain the minimum

(i) SOP expression for the logic circuit,



(5 marks)

(ii) POS expression for the truth table,

R	S	T	U	F
0	0	0	×	1
0	0	1	×	0
0	1	×	×	1
1	0	0	×	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	×	0

(3 marks)

(b) Figure 5(b) represents an adder circuit that takes two-bit binary numbers X_1X_0 and Y_1Y_0 and produces an output binary number Z_1Z_0 and Carry that is equal to the arithmetic addition of the two input numbers.

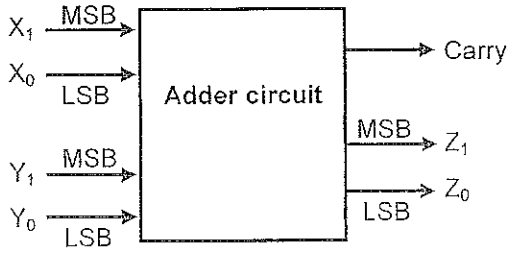


Figure 5(b)

Design the logic circuit for the adder. Show all working clearly. Hint: The logic circuit will have four inputs and three outputs as shown in Table 5(b).

i) Complete the truth table below.

Input X		Input Y		Output Z		Carry
X_1	X_0	Y_1	Y_0	Z_1	Z_0	
0	0	0	0	0	0	0
0	0	0	1	0	1	0
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	0	0	1	1
1	1	1	1	1	0	1

Table 5(b)

(3 marks)

ii) Simplify the Boolean expression to the simplest form using Karnaugh map and/or Boolean algebra for output Z_1, Z_0 and Carry.

(9 marks)

iii) Implement the logic circuit of the simplest Boolean expression for Z_0 using only 2-input NAND gate IC (7400). State the number of IC(s) required for your design.

(5 marks)

Question 6

(a) Figure 6(a) has three inputs (A, B, C) and two outputs (Y, Z).
Table 6a(i) shows a portion of quadruple 2-input AND gates datasheet.
Table 6a(ii) shows a portion of quadruple 2-input OR gates datasheet.
Table 6a(iii) shows a portion of quadruple 2-input XOR gates datasheet.
Table 6a(iv) shows a portion of hex-tuple NOT gates datasheet.

(i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly.

(6 marks)

(ii) What is minimum operating frequency that can be applied to this circuit without affecting the functionality of the circuit? State the function of this circuit.

(4 marks)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	C_L = 15 pF, R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table 6a(i) AND gate

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 6a(ii) OR gate

Symbol	Parameter	Conditions	C_L = 15 pF, R_L = 400Ω		Units
			Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other input LOW		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other input HIGH		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table 6a(iii) XOR gate

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Table 6a(iv) NOT gate

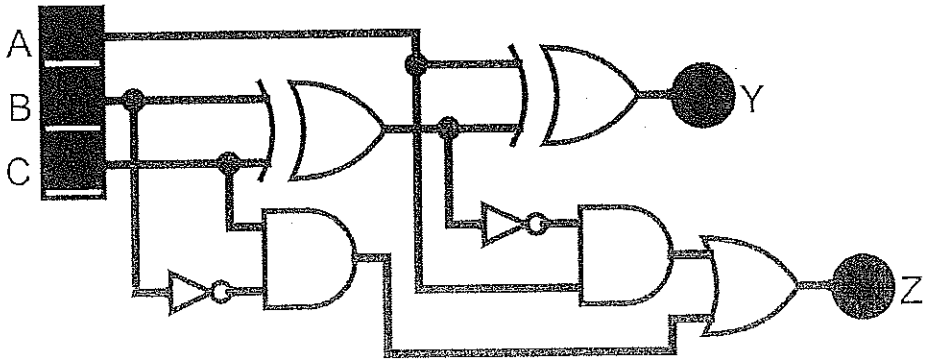


Figure 6(a)

(b) A 12-bit DAC produces an output current in proportion to its digital input. For a digital input of 000010100000, an output current of 75mA is produced.

(i) What will the output current be if the digital input is 100100011110?

(3 marks)

(ii) What is the maximum output current produced by this DAC?

(2 marks)

(iii) What should the digital input be if a 1205mA output current is required?

(2 marks)

(c) Table 6(c) shows the current ratings of TTL series logic gates. A 74F04 NOT gate output is driving 4 (FOUR) Standard TTL gate inputs, 7 (SEVEN) Advanced Low-Power Schottky TTL gate inputs, 3 (THREE) Advanced Schottky TTL gate inputs and 5 (FIVE) Low-Power Schottky TTL gate input as shown in Figure 6(c). Determine if there is a loading problem.

(8 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

Table 6(c)

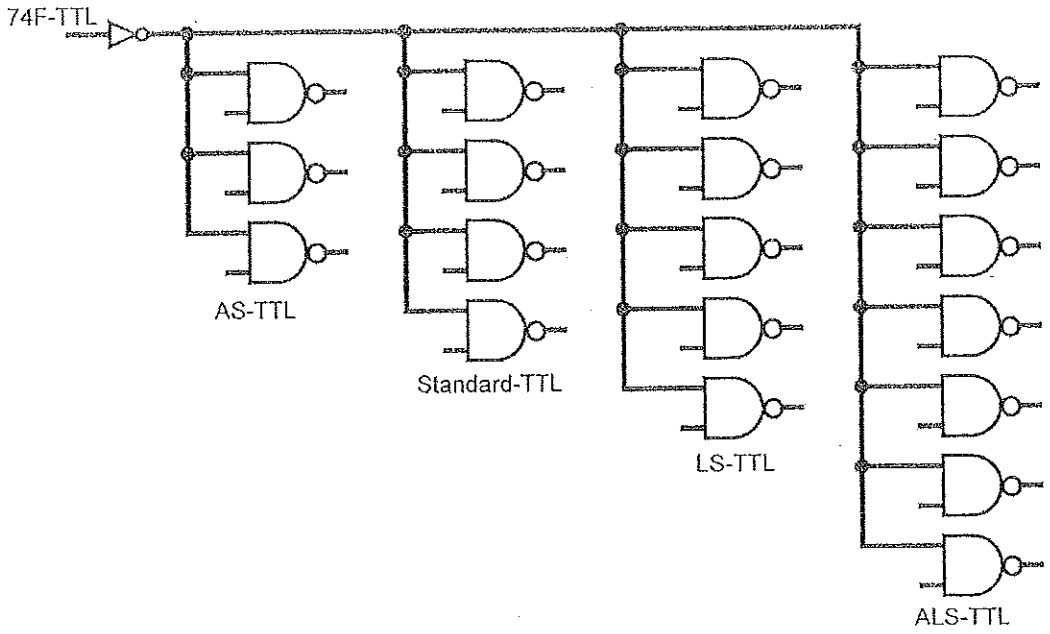


Figure 6(c)

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