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FINAL
Examination Paper

(COVER PAGE)

Session	:	**AUGUST 2016**
Programmes	:	**Diploma in Electrical and Electronic Engineering (DEEI)**
Course	:	**EEE1106: ANALOGUE ELECTRONICS**
Date of Examination	:	5 December 2016 (Monday)
Time	:	8:00am – 10:00am
Duration	:	2 Hours Reading Time : Nil
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : **THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.**

Materials Permitted : Scientific Calculator (Model fx570 Series)

Materials Provided : NIL

Examiner(s) : **Chan Tse Wei**

Moderator : Dr. Khoo Bee Ee

This paper consists of 9 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1106: ANALOGUE ELECTRONICS
FINAL EXAMINATIONS: AUGUST 2016 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. Present your answers neatly and clearly. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

Figure-Q1 shows a JFET based voltage amplifier.

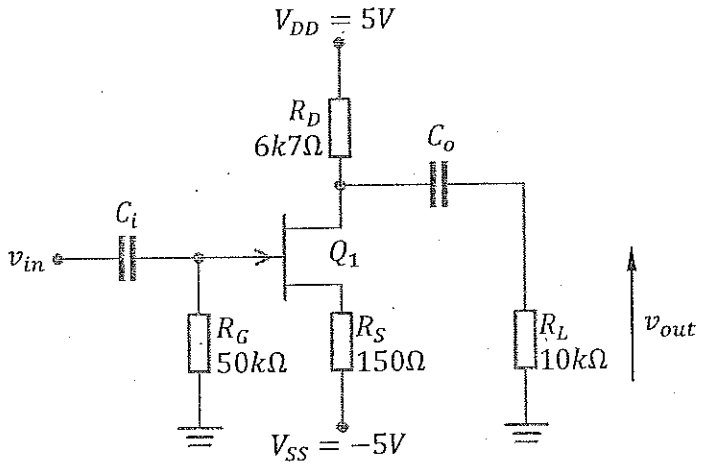

Figure-Q1

a. Qualitatively explain the frequency response characteristics of the amplifier circuit ranging from low to high frequency spectrums, and how users optimize the circuit's performances in terms of voltage amplification. [8]

b. Draw the AC circuit model of the amplifier. Assume that r_d of transistor Q_1 is negligible. [4]

c. Determine the mid-band voltage gain of the amplifier if transistor Q_1 has a transconductance of 50 mS. [5]

d. Determine the percentage of mid-band voltage gain increment if capacitor is connected in parallel with resistor R_S. [3]

e. If the circuit is to be used as a simple audio amplifier, design the circuit such that its lower cutoff frequency is 20 Hz. [5]

Question 2

a. i. Differentiate class A, B and C power amplifiers in terms of their respective transistor conduction period and power conversion efficiency. [6]

ii. State the common approach taken to operate a power transistor under its safe operating area, other than by controlling its electrical quantities. [3]

iii. 20W of DC power is drawn by a power amplifier. If 4W of the power is dissipated as heat by the power transistor and its biasing component, determine the power delivered to the load and the efficiency of the power amplifier. [4]

b. Figure-Q2(b)(i) shows a basic circuit configuration of class B power amplifier, while Figure-Q2(b)(ii) shows an enhanced version of class B power amplifier.

i. State and explain two major problems encountered by the power amplifier in Figure-Q2(b)(i). [4]

ii. Explain how the enhanced version of class B power amplifier eliminates the problems stated in part (b)(i). [6]

iii. State one drawback of the enhanced version of class B power amplifier. [2]

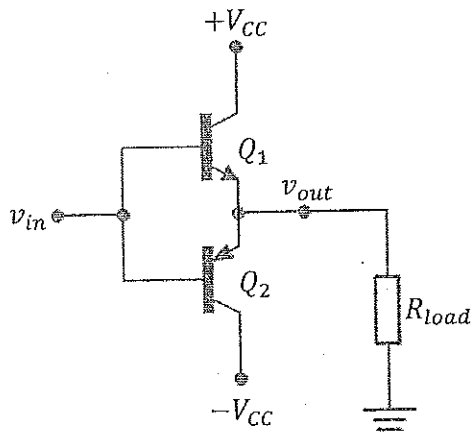

Figure-Q2(b)(i)

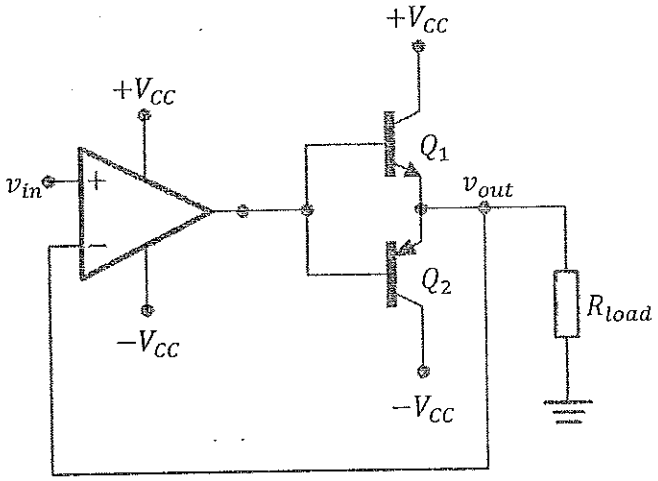

Figure-Q2(b)(ii)

Question 3

a. Figure-Q3(a) shows a basic non-inverting amplifier circuit.

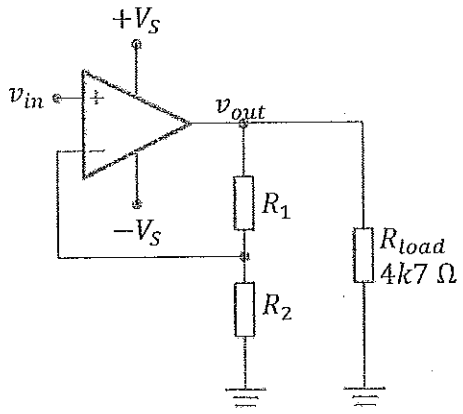

Figure-Q3(a)

i. Derive the voltage gain of the amplifier circuit. Assume that the op-amp has infinite input resistance and zero output resistance. [4]

ii. If the voltage gain of the amplifier circuit needs to be 10, suggest relevant resistance values for resistor R_1 and R_2 for proper practical operation of the op-amp. [4]

iii. If the maximum voltage swing of v_{in} is $\pm 1\ V$ and the voltage gain of the amplifier circuit is 10, suggest practical values of the DC supplies, $\pm V_S$ that will generate an output voltage swing that does not saturate. [2]

b. Figure-Q3(b) shows a AC coupled non-inverting amplifier circuit.

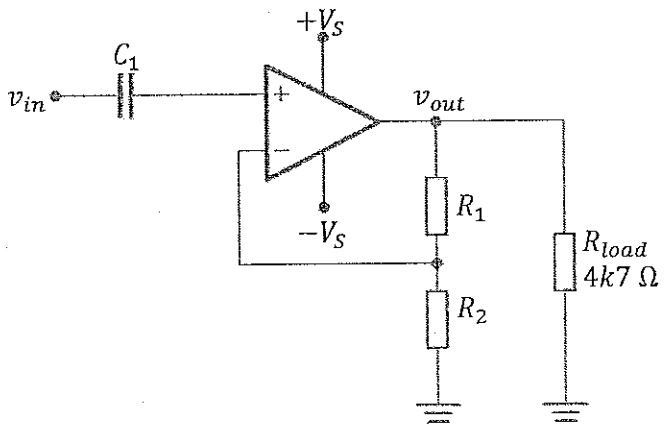

Figure-Q3(b)

i. State the main function of capacitor C_1 in the amplifier circuit. [2]

ii. Explain why the circuit will not operate properly. [3]

iii. Suggest a remedy for the amplifier circuit so that its practical operation is proper. Justify your suggestion. [5]

c. Modify the circuit in Figure-Q3(a) so that the op-amp can be operated in single supply mode with the negative supply terminal grounded. Assume that $v_{in} = V_m \sin(\omega t)$, in which V_m and ω are always within the circuit's operation limits. [5]

Question 4

Figure-Q4 shows an example of Sallen-Key active filter.

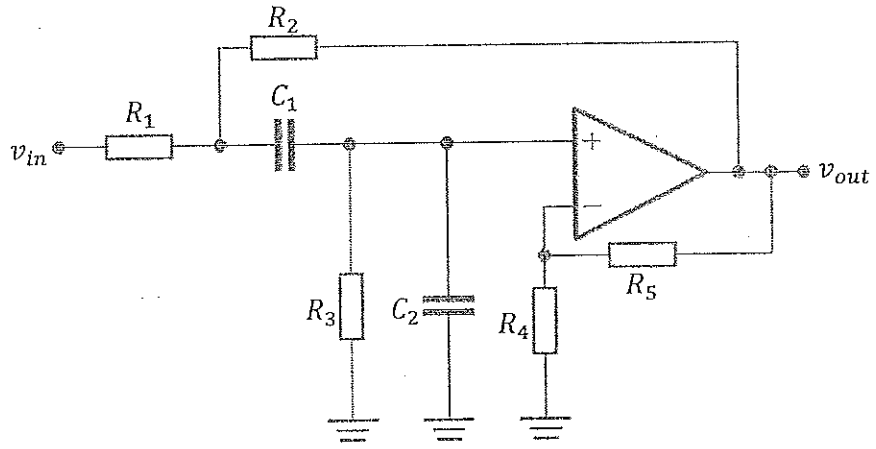

Figure-Q4

a. i. Draw an equivalent circuit configuration for the filter circuit in Figure-Q4 if v_{in} is a DC voltage. Hence, determine the value of the output voltage, v_{out}. [4]

ii. Draw an equivalent circuit configuration for the filter circuit in Figure-Q4 if v_{in} is an AC sinewave with frequency assumed to be infinity. Hence, determine the value of the output voltage, v_{out}. [4]

iii. State the type of filter implemented in Figure-Q4. [2]

b. i. If $R_1 = R_2 = R_3 = R_4 = R_5 = R$ and $C_1 = C_2 = C$ in Figure-Q4, quantitatively derive the active filter's voltage transfer function expression. [8]

ii. Determine the Q-factor of the filter. [5]

iii. Determine the expression of the frequency where maximum voltage gain occurs. [2]

Question 5

a. Figure-Q5(a) shows an improved version of the phase shift oscillator.

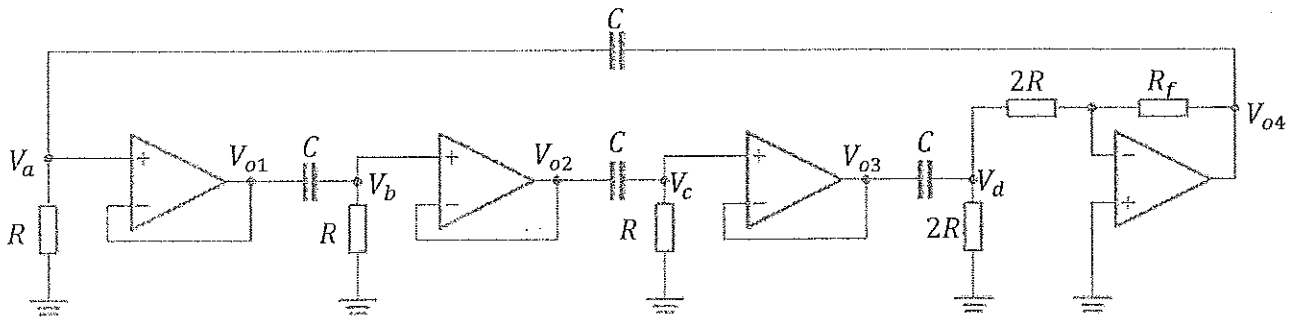

Figure-Q5(a)

i. State the phase shift between V_d and V_{o4}. [2]

ii. To sustain oscillation, state the required phase shift between V_{o4} and V_a. [3]

iii. Explain the purpose of the three buffer circuits in the oscillator. [2]

iv. Derive the relationship of R and C and the frequency of oscillation. [4]

v. Derive the amplifier gain value of the oscillator if oscillation is sustained. [4]

b. Figure-Q5(b) shows a relaxation oscillator constructed from a 555 timer IC.

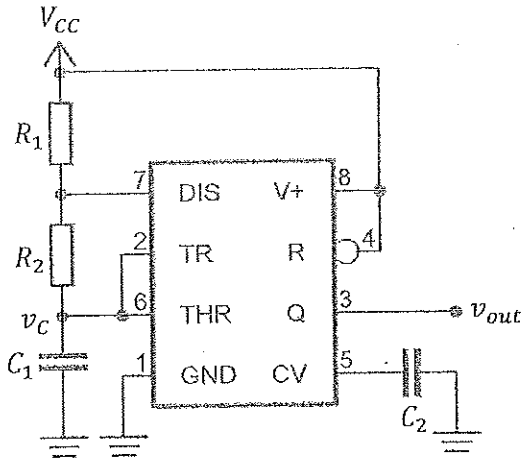

Figure-Q5(b)

i. Sketch the timing diagram of $v_{out}(t)$ and $v_C(t)$ synchronized at the same time scale. [4]

ii. Qualitatively explain why the duty cycle of $v_{out}(t)$ can never be less than 50%. [2]

iii. The oscillation frequency and the duty cycle of the oscillator circuit is given by,

$$f_o = \frac{1}{C_1(R_1 + 2R_2) \times \ln(2)}$$

$$duty\ cycle = \frac{R_1 + R_2}{R_1 + 2R_2}$$

Suggest appropriate practical values for R_1, R_2 and C_1 so that the output waveform oscillates with a frequency of 10 kHz at 70% duty cycle. [4]

Question 6

a. Design a temperature monitoring circuit that will turn on a 5 V buzzer when the ambient temperature exceeds 80°C. The buzzer must remain on until the temperature drops below 30°C. Figure-Q6(a) shows the characteristics of a temperature sensor. Assume all component used in the design are ideal. [12]

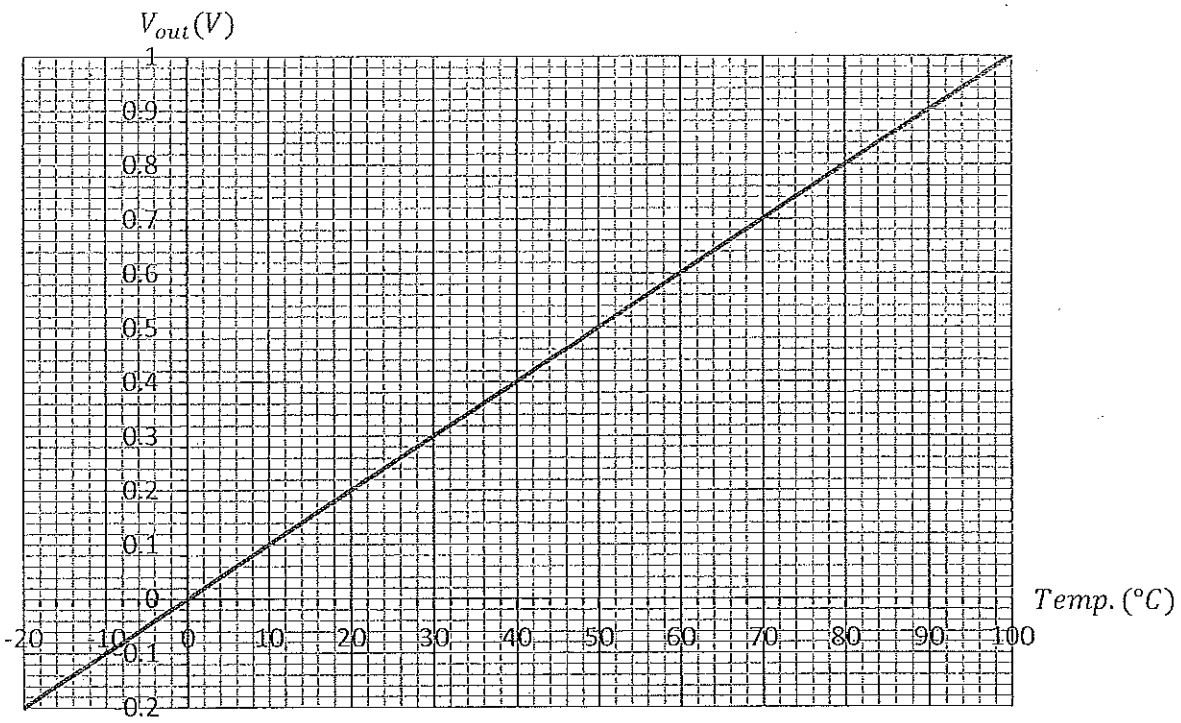

Figure-Q6(a)

b. Figure-Q6(b) shows the frequency response of a low pass active filter.

i. Identify the order of the filter. [2]

ii. Determine the DC gain of the filter in terms of voltage ratio. [3]

iii. Determine the bandwidth of the filter circuit. [2]

iv. Approximate the minimum frequency at which attenuation takes place. [2]

v. Determine the frequency at which $v_{out} = 0.0001v_{in}$. [4]

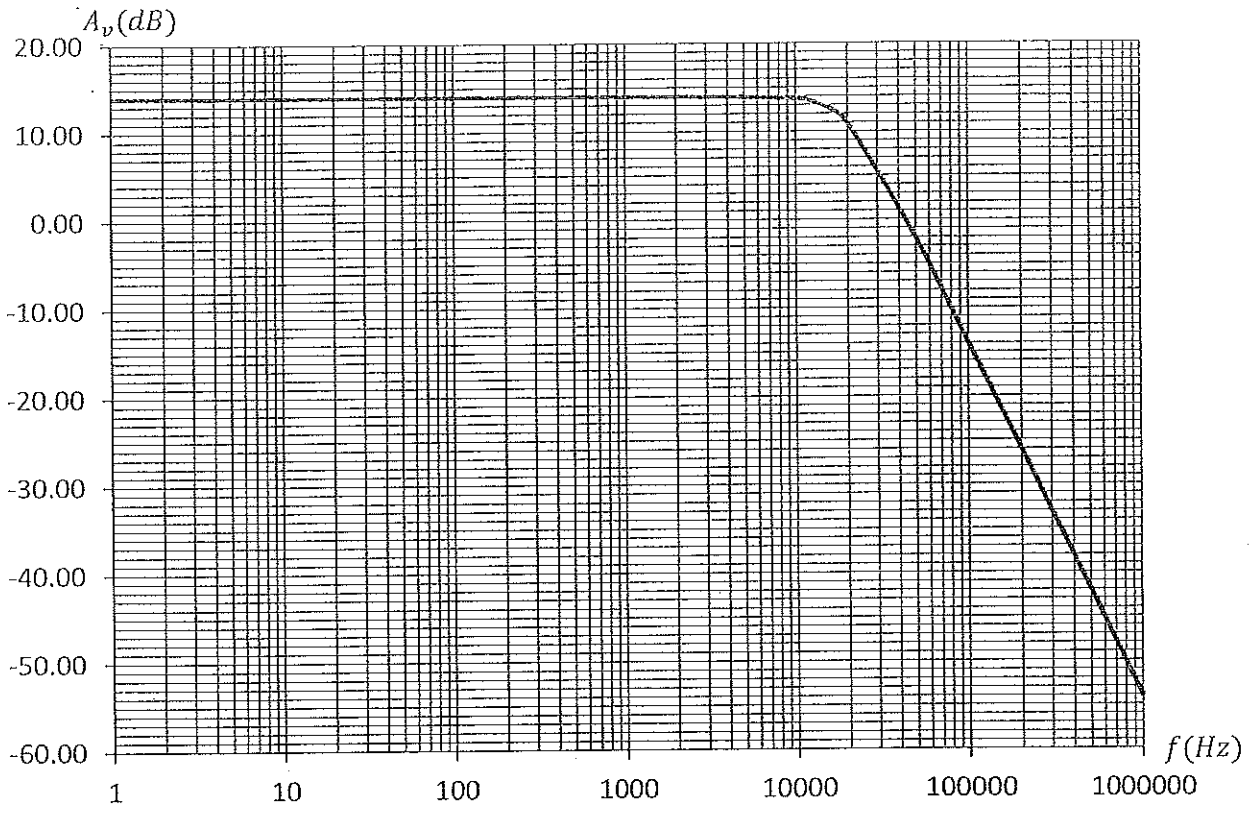

Figure-Q6(b)

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