INTI
International College Penang
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session : **August 2015**

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : **EEE2105: Introduction to Microprocessors**

Date of Examination : 6th December 2015 (Sunday)

Time : 8:00 am – 10:00 am

Duration : 2 Hours Reading Time : Nil

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials Permitted :

Nil

Materials Provided :

Appendix A,B,C,D & E

Examiner(s) : **Mr. Steven Khoo Boo Tap**

Moderator : Dr. Mandeep Singh

This paper consists of 12 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2105: INTRODUCTION TO MICROPROCESSORS
FINAL EXAMINATION: AUG2015 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Calculate the address range for these outputs Y1, Y4 and Y7 of the 74LS138 active-low decoder for the design shown in Figure 1(a).

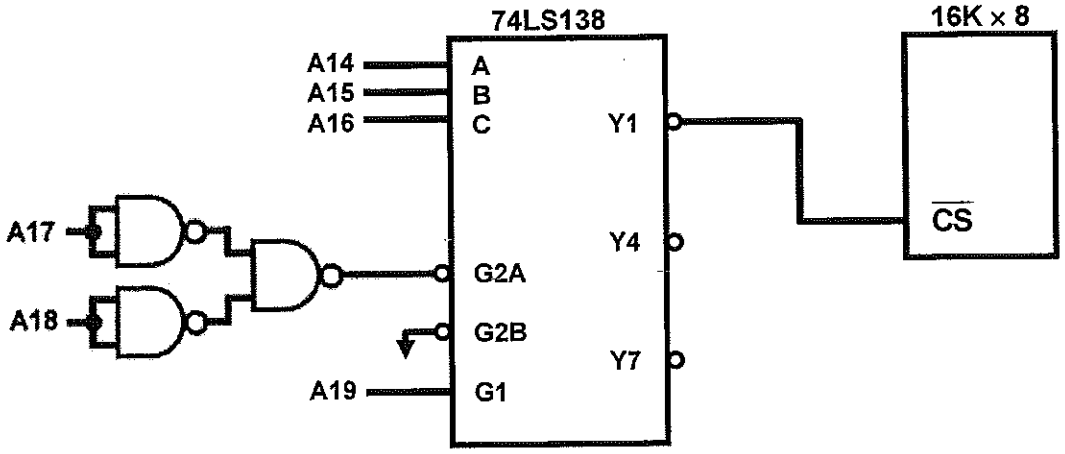


Figure 1(a)

(7 marks)

(b) Comment on the validity of the following instructions. For those invalid instructions, explain why. For those valid instructions, state the addressing mode.

(i) MOV BX, [AX]

(2 marks)

(ii) MOV DL, [BP][BX][DI][SI] 22H

(2 marks)

(iii) MOV CS, DS

(2 marks)

(iv) MOV CL, [BX+0AH]

(2 marks)

(c) Perform the following number system transformation. Show all workings clearly.

(i) $A4.F4_{16}$ to decimal equivalent with 6 decimal points accuracy.

(2 marks)

(ii) $[10215.01_8 \times 12_8]$ to hexadecimal equivalent with 2 hexadecimal points accuracy.

(4 marks)

(iii) $[164.953125_{10} - 11.101_{16}]$ to binary equivalent with 12 binary points accuracy.

(4 marks)

Question 2

(a) Explain the term of the following with an appropriate diagram.

(i) Simplex

(3 marks)

(ii) Half-Duplex

(3 marks)

(iii) Full-Duplex

(3 marks)

(b) At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal)

Registers

	H	L
AX	2C	10
BX	00	14
CX	10	01
DX	2B	33
CS	02	00
DS	90	00
SS	40	10
ES	61	00
BP	00	1F
SP	00	05
IP	11	0B
SI	21	34
DI	FF	FF

Memory

9000B	12
9000A	34
90009	56
90008	78
90007	9A
90006	BA
90005	DE
90004	F0
90003	21
90002	43
90001	09
90000	67
8FFFF	54
8FFFE	DF

4010E	6F
4010D	2D
4010C	C1
4010B	25
4010A	3F
40109	12
40108	FF
40107	FC
40106	E1
40105	10
40104	00
40103	36
40102	21
40101	88

(i) What is the physical address of the next instruction to be executed?

(2 marks)

(ii) What is the physical address of the top of the stack?

(2 marks)

(iii) Draw a memory map for the 8086 microprocessor, indicating clearly the start and end addresses of the segments.

(3 marks)

(iv) Provide the registers and memory locations that are effected, and their new values after the execution of ADD [BX – 0EH], AX, also state the number of bytes used for this instruction.

(3 marks)

(c) What is the different between JMP (Unconditional Jump) and CALL (Unconditional Call) instructions? Provide FOUR (4) detail comparisons.

Illustrate clearly using an appropriate example to show the differences. Use same data for the comparison of both the instruction.

(6 marks)

Question 3

(a) A 10-MHz 8086 based system is using ROM of 650-ns speed. Calculate the number of wait states that the ROM selection circuitry must add if the delay due to data path and decoding circuitry (74LS138, and so on) is 35-ns.

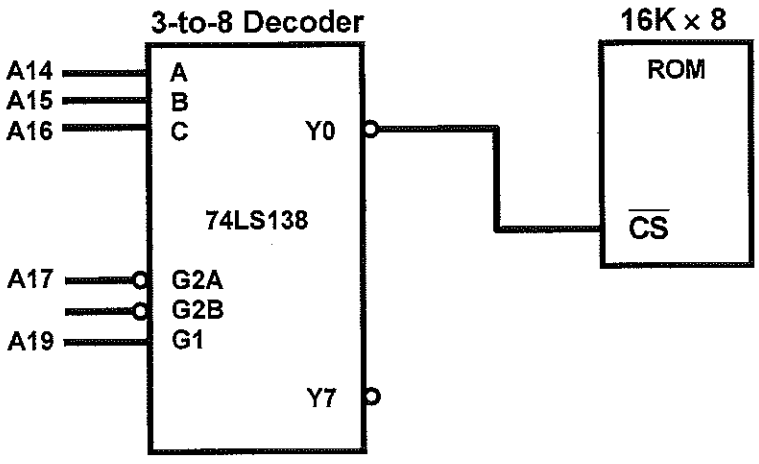


Figure 3(a) 8086 Based System

(5 marks)

(b) The 8255 PPI is configured as shown in Figure 3(b). Write a program to count the number of 'zeroes" in the incoming data received from port C continuously via 8255 PPI. The results will be sent to port A if the count result is even and sent to port B if the count result is odd. Assume the configuration below is using Mode 0.

Also, include comments for any instruction used. The program length should be as minimum as possible.

(12 marks)

Examples of incoming data and the respective action:

- 25_H (**00100101**) ⇨ send 05_H (Odd) out to port B
- CC_H (**11001100**) ⇨ send 04_H (Even) out to port A
- 00_H (**00000000**) ⇨ send 08_H (Even) out to port A
- EF_H (**11101111**) ⇨ send 01_H (Odd) out to port B
- FF_H (**11111111**) ⇨ send 00_H (Even) out to port A
- 73_H (**01110011**) ⇨ send 03_H (Odd) out to port B

[Refer to Appendix C for 8255 PPI Control Word]

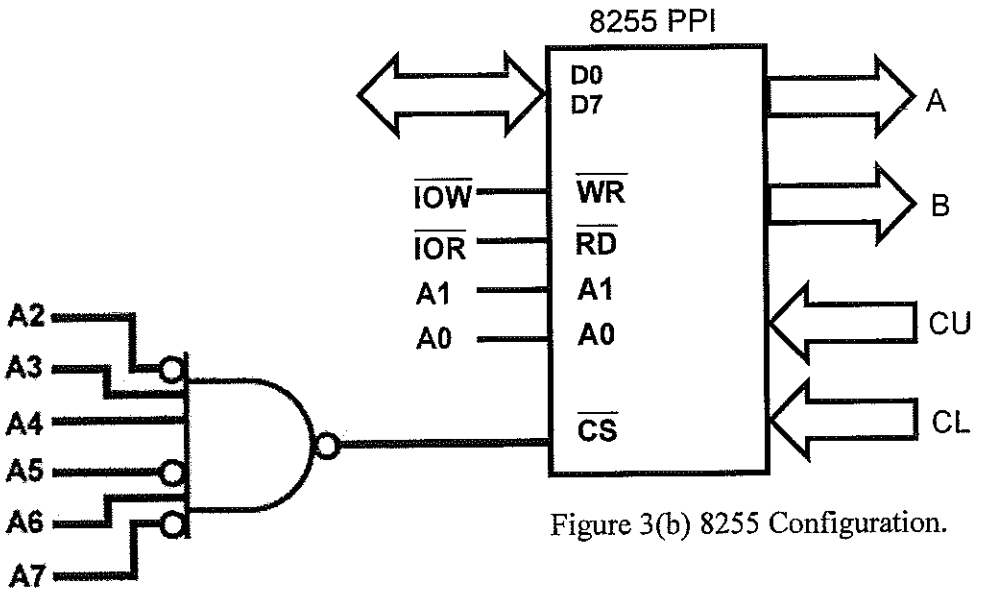


Figure 3(b) 8255 Configuration.

(c) Describe the function of the following pins of 8086 microprocessors.

(i) RESET [pin 21]

(2 marks)

(ii) READY [pin 22]

(2 marks)

(iii) NMI [pin 17]

(2 marks)

(iv) INTR [pin 18]

(2 marks)

Question 4

(a) Given the registers and the memory locations contents of 8086 as follows: (All values are in Hexadecimal).

Registers					
AX	1234H	CS	3010H	DI	0555H
BX	0404H	DS	5F41H	SI	5060H
CX	5678H	SS	5F81H	BP	6070H
DX	789AH	ES	7040H	IP	7100H

Figure 4(a-1) Registers and the content

Memory																
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
5F800H	11	22	33	44	55	66	77	88	99	00	A1	B1	C1	D1	E1	F1
5F810H	02	04	45	78	90	11	22	33	44	55	66	77	88	99	00	12
5F820H	34	56	78	90	12	34	56	78	90	12	34	56	78	90	11	22
5F830H	33	44	55	66	77	88	99	00	10	A0	12	34	56	78	9A	BC
5F840H	DE	F0	00	11	00	11	10	21	99	B8	77	33	58	45	33	22
5F850H	25	31	19	00	01	22	20	31	89	C8	66	22	CC	54	44	06
5F860H	DC	F0	20	18	02	33	30	41	79	D8	55	11	BB	67	55	20
5F870H	FE	F1	10	12	03	44	40	51	69	E8	44	AA	55	76	66	21
5F880H	00	FF	00	FF	00	FF	00	60	5F	FF	14	00	FF	F1	80	09

Figure 4(a-2) Memory locations and the content

Perform the following operations. Indicate the result in the register and the content where it is stored. The operations are independent of each other. Show all workings of before and after with appropriate diagram illustration.

(i) SUB [0416H – 32], DX

(3 marks)

(ii) XOR [BP] + 23 + 23H – 60213o, BH

(3 marks)

(iii) AND [DI] + 101b + 101o – 101 – 101H, AX

(3 marks)

(iv) ADD [SI + BP + 0EB0H – BFADH + 10010000b], CX

(3 marks)

(b) Calculate the time delay taken for the program in Figure 4(b-2) running on 8086 microprocessor at 10-MHz. At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal).

Assume that DS register contains 0700H. Show all workings clearly for each instruction.

(13 marks)

[Refer to Appendix A for the cycle time]

	Memory															
	00	**01**	**02**	**03**	**04**	**05**	**06**	**07**	**08**	**09**	**0A**	**0B**	**0C**	**0D**	**0E**	**0F**
07700H	08	04	45	78	10	21	22	33	34	25	26	27	28	49	40	14
07800H	02	03	05	01	12	24	56	01	16	00	34	56	98	50	19	62
07900H	07	20	30	40	50	60	70	80	90	02	00	C0	D0	E0	F0	00
07A00H	1D	1C	1B	1A	19	18	55	66	47	46	05	44	43	42	41	0F
07B00H	18	19	23	48	25	26	27	58	29	31	32	35	36	37	38	39

Figure 4(b-1) Random Address Memory

Program		
	MOV	AL, 02H
LOOP4:	MOV	BL, [0A0AH]
LOOP3:	MOV	DX, [0808H]
LOOP2:	MOV	CX, [0909H]
LOOP1:	NOP	
	NOP	
	LOOP	LOOP1
	DEC	DL
	JNZ	LOOP2
	NOP	
	DEC	BL
	JNZ	LOOP3
	XOR	AL, AL
	JNZ	LOOP4
	HLT	

Figure 4(b-2) Coding.

Question 5

(a) A 10-MHz 8086 microprocessor is interfacing with a 3-MHz 8237 DMA. The CPU bus cycle uses one wait state and the bus cycle for the DMA is 4 clocks. Calculate the DMA data transfer rate if the system bus is used alternately by the CPU and DMA. Express the answer in Kbytes/s.

(6 marks)

(b) A transmission system uses three asynchronous serial data communication settings to transmit a passcode that contain 9 characters to the receiver via 8250 UART chip. Figure 5(b-1) is used to transmit the first 3 characters, followed by Figure 5(b-2) setting for the next 4 characters and finally, Figure 5(b-3) setting for the last 2 characters of the transmission.

The **LSB** is transmitted first.

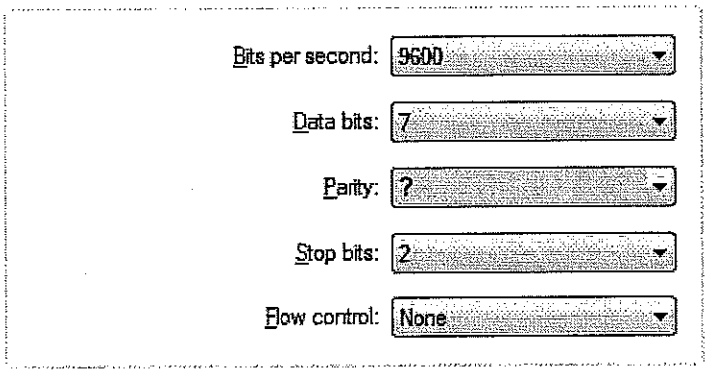


Figure 5(b-1) First 3 characters setting.

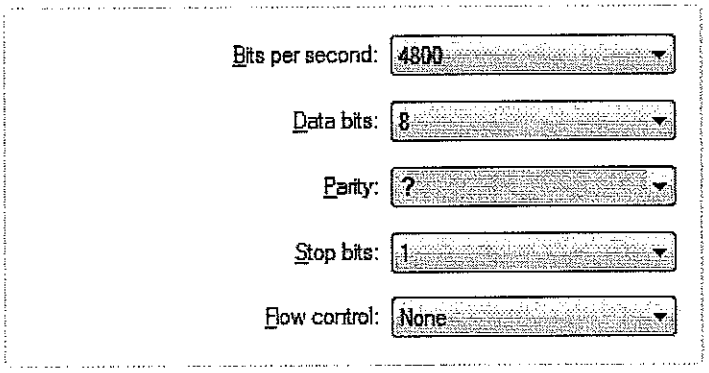


Figure 5(b-2) Next 4 characters setting.

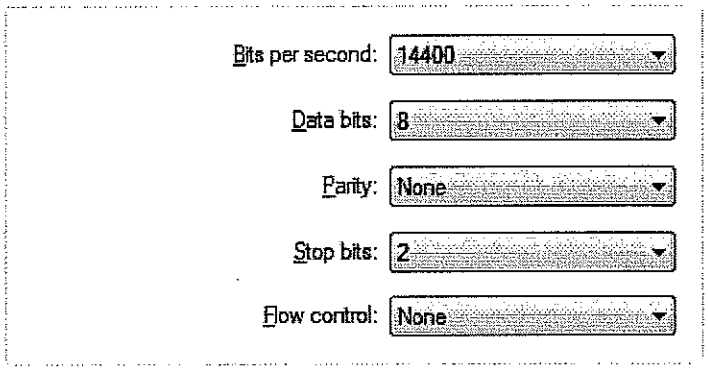


Figure 5(b-3) Last 2 characters setting.

Decode the following serial data received in continuous ASCII characters message:
Incoming data:
01110110111001011111110101101001100001110001010111100010100111001100101111001001101111110110011 0011

(i) What is the passcode transmitted and passcode solution?

(10 marks)

(ii) What is the Parity setting used for Figure 5(b-1) and Figure 5(b-2)?

(2 marks)

(iii) Calculate the total time when transmitting the above message and the time wasted due to overhead.

(3 marks)

[Refer to Appendix B for ASCII codes]

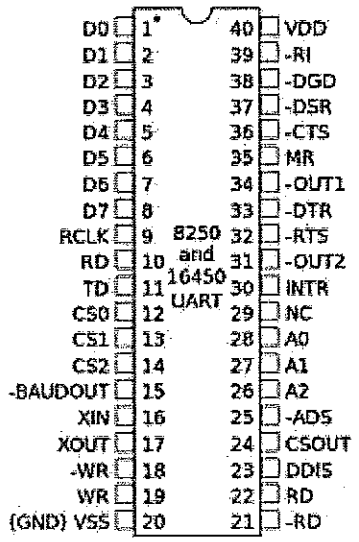


Figure 5(b-4) 8250 UART pin configuration.

(c) The 8259 PIC is configured as shown in Figure 5(c). Write a program to initialize the 8259 using the port addresses in Figure 5(c). Assume the ICW1 is 1BH, ICW2 is 58H, no ICW3 and ICW4 is 2FH. Also include comments for any instruction used.

(4 marks)

[Refer to Appendix E for 8259 PIC Control Words]

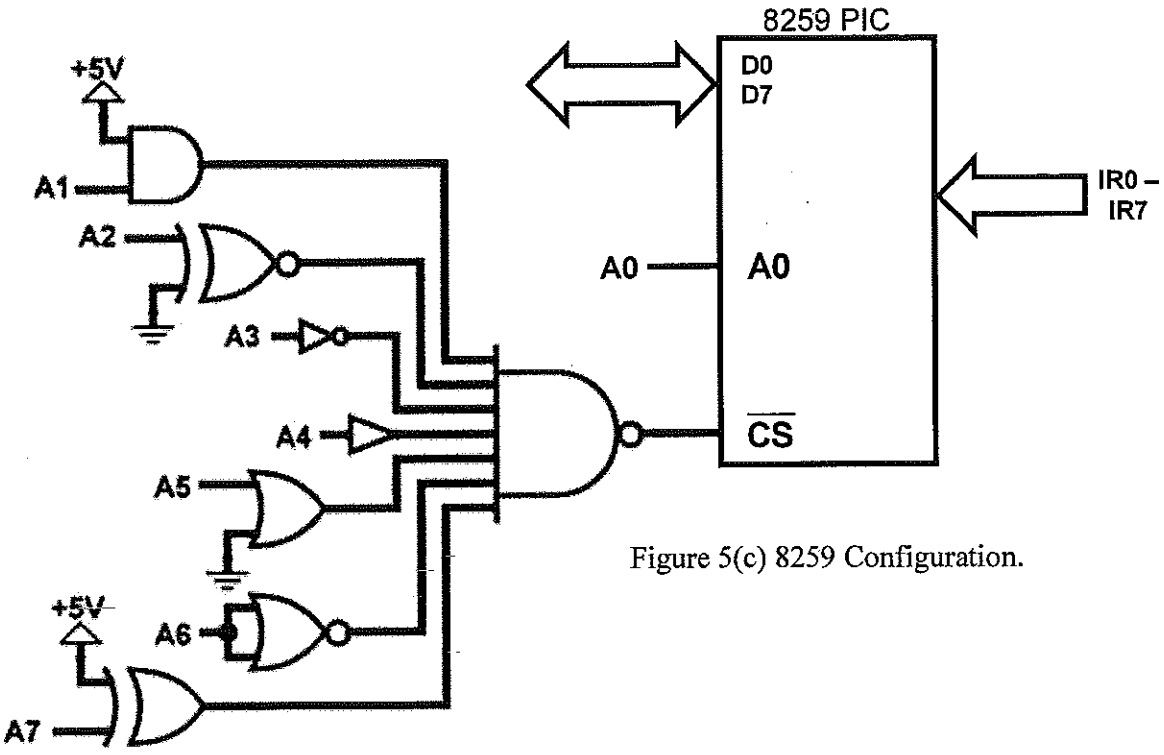


Figure 5(c) 8259 Configuration.

Question 6

(a) Figure 6(a-1) shows a TM4100GAD8 Dynamic RAM Module pin configuration. Figure 6(a-2) shows a TM497GU8 Dynamic RAM Module pin configuration.

Determine the:

(i) total memory capacity of the area (A and B) memory device in Kbits,

(4 marks)

(ii) individual memory organization,

(2 marks)

(iii) number of address pins and number of data pins of each memory device.

(4 marks)

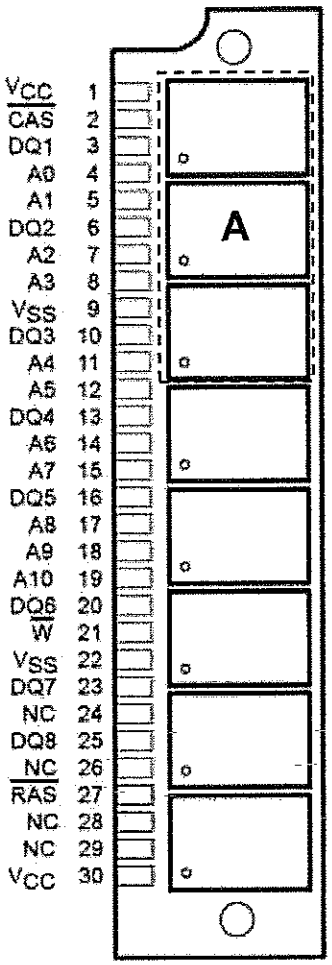


Figure 6(a-1) TM4100GAD8 DRAM Module pin configuration.

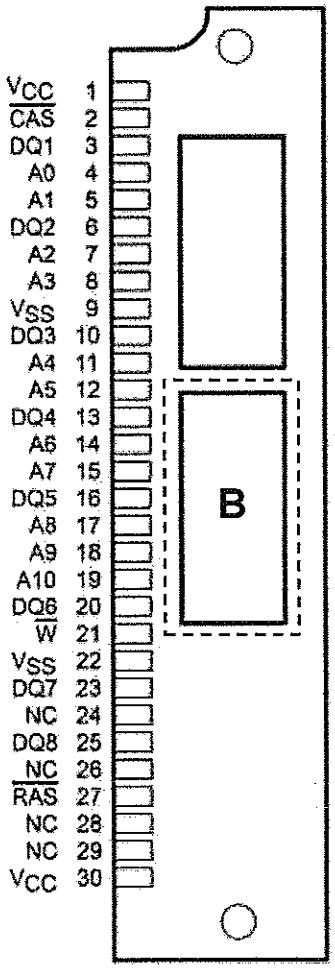


Figure 6(a-2) TM497GU8 DRAM Module pin configuration.

(b) With the aid of a suitable diagram with details labelling, illustrate step-by-step how DMA can be used to speed up CPU operation during the transfer of data from memory to an I/O device.

The diagram should include the control signals for Microprocessor (CPU), DMA, Memory and I/O Device. The steps describe should be as detail as possible describing all control signals operation.

(10 marks)

(c) The 8254 PIT chip is configured as shown in Figure 6(c). CLK1 of counter 1 is 1.19318-MHz and Gate1 is connected to high permanently. Counter 1 generates a periodic pulse every 45.2573-μs to refresh DRAM memory of the computer. Write assembly instructions to generate this periodic pulse through OUT1.

(5 marks)

[Refer to Appendix D for 8253/8254 PIT Control Word]

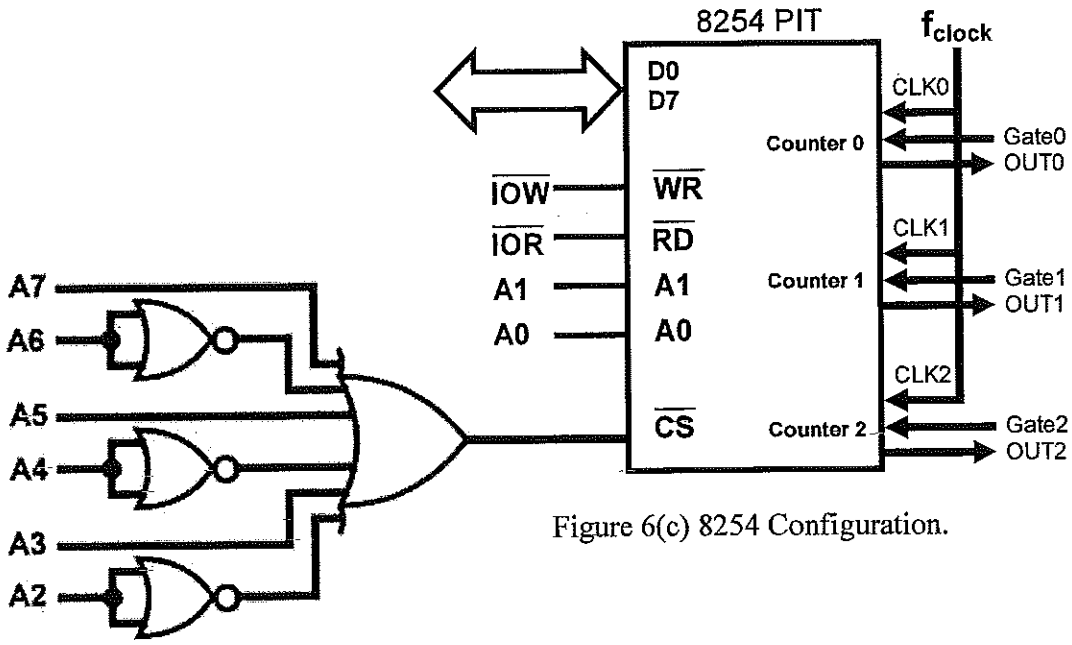


Figure 6(c) 8254 Configuration.

– THE END –

EEE2105(F)/Aug15/Steven Khoo/12/08/15

APPENDIX A: 8086 INSTRUCTION SET SUMMARY

Instruction Set Summary

Mnemonic	Description	Clock cycles	Number of bytes	Flags O D I T S Z A P C	Page ref.
AAA	ASCII adjust for addition	4	1	u - - - u u x u x	76
AAD	ASCII adjust for division	60	2	u - - - x x u x u	76
AAM	ASCII adjust for multiplication	83	2	u - - - x x u x u	76
AAS	ASCII adjust for subtraction	4	1	u - - - u u x u x	76
ADC	Add with carry			x - - - x x x x x	65
	Register to register	3	2		
	Memory to register	9+EA	2–4		
	Register to memory	16+EA	2–4		
	Immediate to register	4	3–4		
	Immediate to memory	17+EA	3–6		
	Immediate to accumulator	4	2–3		
ADD	Addition			x - - - x x x x x	65
	Register to register	3	2		
	Memory to register	9+EA	2–4		
	Register to memory	16+EA	2–4		
	Immediate to register	4	3–4		
	Immediate to memory	17+EA	3–6		
	Immediate to accumulator	4	2–3		
AND	Logical AND			0 - - - x x u x 0	93
	Register to register	3	2		
	Memory to register	9+EA	2–4		
	Register to memory	16+EA	2–4		
	Immediate to register	4	3–4		
	Immediate to memory	17+EA	3–6		
	Immediate to accumulator	4	2–3		
CALL	Call a procedure			- - - - - - - - -	157
	Intrasegment direct	19	3		
	Intrasegment indirect through register	16	2		
	Intrasegment indirect through memory	21+EA	2–4		
	Intersegment direct	28	5		
	Intersegment indirect	37+EA	2–4		
CBW	Convert byte to word	2	1	- - - - - - - - -	68
CLC	Clear carry flag	2	1	- - - - - - - - 0	92
CLD	Clear direction flag	2	1	- 0 - - - - - - -	92
CLI	Clear interrupt flag	2	1	- - 0 - - - - - -	92
CMC	Complement carry flag	2	1	- - - - - - - - x	92
CMP	Compare			x - - - x x x x x	69
	Register to register	3	2		
	Memory to register	9+EA	2–4		
	Register to memory	9+EA	2–4		
	Immediate to register	4	3–4		
	Immediate to memory	10+EA	3–6		

Mnemonic	Description	Clock cycles	Number of bytes	Flags O D I T S Z A P C	Page ref.
	Immediate to accumulator	4	2–3		
CMPS/	Compare string/		1	x - - - x x x x x	208
CMPSB/	Compare byte string/				
CMPSW	Compare word string				
	Not repeated	22			
	Repeated	9+22/rep			
CWD	Convert word to double word	5	1	- - - - - - - - -	68
DAA	Decimal adjust for addition	4	1	u - - - x x x x x	74
DAS	Decimal adjust for subtraction	4	1	u - - - x x x x x	74
DEC	Decrement by 1			x - - - x x x x -	69
	16-bit register	2	1		
	8-bit register	3	2		
	Memory	15+EA	2–4		
DIV	Unsigned division			u - - - u u u u u	70
	8-bit register	80–90	2		
	16-bit register	144–162	2		
	8-bit memory	(86–96) +EA	2–4		
	16-bit memory	(150–168) +EA	2–4		
ESC	Escape			- - - - - - - - -	457
	Register	2	2		
	Memory	8+EA	2–4		
HLT	Halt	2	1	- - - - - - - - -	91
IDIV	Integer division			u - - - u u u u u	70
	8-bit register	101–112	2		
	16-bit register	165–184	2		
	8-bit memory	(107–118) +EA	2–4		
	16-bit memory	(171–190) +EA	2–4		
IMUL	Integer multiplication			x - - - u u u u x	70
	8-bit register	80–98	2		
	16-bit register	128–154	2		
	8-bit memory	(86–104) +EA	2–4		
	16-bit memory	(134–160) +EA	2–4		
IN	Input from I/O port			- - - - - - - - -	232
	Fixed port	10	2		
	Variable port	8	1		
INC	Increment by 1			x - - - x x x x -	69
	16-bit register	2	1		
	8-bit register	3	2		
	Memory	15+EA	2–4		
INT	Interrupt			- - 0 0 - - - - -	172

Mnemonic	Description	Clock cycles	Number of bytes	Flags O D I T S Z A P C	Page ref.
	Type = 3	52	1		
	Type ≠ 3	51	2		
INTO	Interrupt if overflow		1	- - 0 0 - - - - -	172
	Interrupt is taken	53			
	Interrupt is not taken	4			
IRET	Return from interrupt	24	1	r r r r r r r r r	172
JA/	Jump if above/	16/4	2	- - - - - - - - -	80
JNBE	Jump if not below or equal				
JAE/	Jump if above or equal/	16/4	2	- - - - - - - - -	80
JNB/	Jump if not below/				
JNC	Jump if not carry				
JB/	Jump if below/	16/4	2	- - - - - - - - -	80
JNAE/	Jump if not above or equal/				
JC	jump if carry				
JBE/	Jump if below or equal/	16/4	2	- - - - - - - - -	80
JNA	Jump if not above				
JCXZ	Jump if CX is zero	18/6	2	- - - - - - - - -	88
JE/	Jump if equal/	16/4	2	- - - - - - - - -	80
JZ	Jump if zero				
JG/	Jump if greater/	16/4	2	- - - - - - - - -	80
JNLE	Jump if not less or equal				
JGE/	Jump if greater or equal/	16/4	2	- - - - - - - - -	80
JNL	Jump if not less				
JL/	Jump if less/	16/4	2	- - - - - - - - -	80
JNGE	Jump if not greater or equal				
JLE/	Jump if less or equal/	16/4	2	- - - - - - - - -	80
JNG	Jump if not greater				
JMP	Jump			- - - - - - - - -	84
	Intrasegment direct short	15	2		
	Intrasegment direct	15	3		
	Intersegment direct	15	5		
	Intrasegment indirect through memory	18 + EA	2–4		
	Intrasegment indirect through register	11	2		
	Intersegment indirect	24 + EA	2–4		
JNE/	Jump if not equal/	16/4	2	- - - - - - - - -	80
JNZ	Jump if not zero				
JNO	Jump if not overflow	16/4	2	- - - - - - - - -	80
JNP/	Jump if not parity/	16/4	2	- - - - - - - - -	80
JPO	Jump if parity odd				
JNS	Jump if not sign	16/4	2	- - - - - - - - -	80
JO	Jump if overflow	16/4	2	- - - - - - - - -	80
JP/	Jump if parity/	16/4	2	- - - - - - - - -	80
JPE	Jump if parity even				
JS	Jump if sign	16/4	2	- - - - - - - - -	80
LAHF	Load AH from flags	4	1	- - - - - - - - -	92
LDS	Load pointer using DS	16 + EA	2–4	- - - - - - - - -	60
LEA	Load effective address	2 + EA	2–4	- - - - - - - - -	60

Mnemonic	Description	Clock cycles	Number of bytes	Flags O D I T S Z A P C	Page ref.
LES	Load pointer using ES	16+EA	2–4	- - - - - - - - - -	60
LOCK	Lock bus	2	1	- - - - - - - - - -	455
LODS/	Load string/		1	- - - - - - - - - -	208
LODSB/	Load byte string/				
LODSW	Load word string				
	Not repeated	12			
	Repeated	9+13/rep			
LOOP	Loop	17/5	2	- - - - - - - - - -	88
LOOPE/	Loop if equal/	18/6	2	- - - - - - - - - -	88
LOOPZ	Loop if zero				
LOOPNE/	Loop if not equal/	19/5	2	- - - - - - - - - -	88
LOOPNZ	Loop if not zero				
MOV	Move			- - - - - - - - - -	60
	Accumulator to memory	10	3		
	Memory to accumulator	10	3		
	Register to register	2	2		
	Memory to register	8+EA	2–4		
	Register to memory	9+EA	2–4		
	Immediate to register	4	2–3		
	Immediate to memory	10+EA	3–6		
	Register to SS, DS, or ES	2	2		
	Memory to SS, DS, or ES	8+EA	2–4		
	Segment register to register	2	2		
	Segment register to memory	9+EA	2–4		
MOVS/	Move string/		1	- - - - - - - - - -	208
MOVSB/	Move byte string/				
MOVSW	Move word string				
	Not repeated	18			
	Repeated	9+17/rep			
MUL	Unsigned multiplication			x - - - u u u u x	70
	8-bit register	70–77	2		
	16-bit register	118–133	2		
	8-bit memory	(76–83) +EA	2–4		
	16-bit memory	(124–139) +EA	2–4		
NEG	Negate			x - - - x x x x x	69
	Register	3	2		
	Memory	16+EA	2–4		
NOP	No operation	3	1	- - - - - - - - - -	91
NOT	Logical NOT			- - - - - - - - - -	93
	Register	3	2		
	Memory	16+EA	2–4		
OR	Logical OR			0 - - - x x u x 0	93
	Register to register	3	2		
	Memory to register	9+EA	2–4		
	Register to memory	16+EA	2–4		

Mnemonic	Description	Clock cycles	Number of bytes	Flags O D I T S Z A P C	Page ref.
	Immediate to accumulator	4	2–3		
	Immediate to register	4	3–4		
	Immediate to memory	17+EA	3–6		
OUT	Output to I/O port			- - - - - - - - - -	232
	Fixed port	10	2		
	Variable port	8	1		
POP	Pop word off stack			- - - - - - - - - -	153
	Register	8	1		
	Segment register SS, DS, or ES	8	1		
	Memory	17+EA	2–4		
POPF	Pop flags off stack	8	1	r r r r r r r r r	153
PUSH	Push word onto stack			- - - - - - - - - -	153
	Register	11	1		
	Segment register	10	1		
	Memory	16+EA	2–4		
PUSHF	Push flags onto stack	10	1	- - - - - - - - - -	153
RCL	Rotate left through carry			x - - - - - - - - x	98
	Register with single-shift	2	2		
	Register with variable-shift	8+4/bit	2		
	Memory with single-shift	15+EA	2–4		
	Memory with variable-shift	20+EA +4/bit	2–4		
RCR	Rotate right through carry			x - - - - - - - - x	98
	Register with single-shift	2	2		
	Register with variable-shift	8+4/bit	2		
	Memory with single-shift	15+EA	2–4		
	Memory with variable-shift	20+EA +4/bit	2–4		
REP	Repeat string operation	2	1	- - - - - - - - - -	213
REPE/	Repeat operation while equal/	2	1	- - - - - - - - - -	213
REPZ	Repeat operation while zero				
REPNE/	Repeat operation while not equal/	2	1	- - - - - - - - - -	213
REPNZ	Repeat operation while not zero				
RET	Return from procedure			- - - - - - - - - -	157
	Intrasegment	8	1		
	Intrasegment with constant	12	3		
	Intersegment	18	1		
	Intersegment with constant	17	3		
ROL	Rotate left			x - - - - - - - - x	98
	Register with single-shift	2	2		

Mnemonic	Description	Clock cycles	Number of bytes	Flags O D I T S Z A P C	Page ref.
	Register with variable-shift	8+4/bit	2		
	Memory with single-shift	15+EA	2–4		
	Memory with variable-shift	20+EA +4/bit	2–4		
ROR	Rotate right			x - - - - - - - x	98
	Register with single-shift	2	2		
	Register with variable-shift	8+4/bit	2		
	Memory with single-shift	15+EA	2–4		
	Memory with variable-shift	20+EA +4/bit	2–4		
SAHF	Store AH into flags	4	1	- - - - r r r r r	92
SAL/	Shift arithmetic left/			x - - - x x u x x	98
SHL	Shift logical left				
	Register with single-shift	2	2		
	Register with variable-shift	8+4/bit	2		
	Memory with single-shift	15+EA	2–4		
	Memory with variable-shift	20+EA +4/bit	2–4		
SAR	Shift arithmetic right			x - - - x x u x x	98
	Register with single-shift	2	2		
	Register with variable-shift	8+4/bit	2		
	Memory with single-shift	15+EA	2–4		
	Memory with variable-shift	20+EA +4/bit	2–4		
SBB	Subtract with borrow			x - - - x x x x x	65
	Register from register	3	2		
	Memory from register	9+EA	2–4		
	Register from memory	16+EA	2–4		
	Immediate from accumulator	4	2–3		
	Immediate from register	4	3–4		
	Immediate from memory	17+EA	3–6		
SCAS/	Scan string/		1	x - - - x x x x x	208
SCASB/	Scan byte string/				
SCASW	Scan word string				
	Not repeated	15			
	Repeated	9+15/rep			
SHR	Shift logical right			x - - - x x u x x	98
	Register with single-shift	2	2		
	Register with variable-shift	8+4/bit	2		
	Memory with single-shift	15+EA	2–4		
	Memory with variable-shift	20+EA +4/bit	2–4		
STC	Set carry flag	2	1	- - - - - - - - 1	92
STD	Set direction flag	2	1	- 1 - - - - - - -	92

Mnemonic	Description	Clock cycles	Number of bytes	Flags O D I T S Z A P C	Page ref.
STI	Set interrupt flag	2	1	- - 1 - - - - - -	92
STOS/	Store string/		1	- - - - - - - - -	208
STOSB/	Store byte string/				
STOSW	Store word string				
	Not repeated	11			
	Repeated	9+10/rep			
SUB	Subtraction			x - - - x x x x x	65
	Register from register	3	2		
	Memory from register	9+EA	2–4		
	Register from memory	16+EA	2–4		
	Immediate from accumulator	4	2–3		
	Immediate from register	4	3–4		
	Immediate from memory	17+EA	3–6		
TEST	Test			0 - - - x x u x 0	93
	Register with register	3	2		
	Memory with register	9+EA	2–4		
	Immediate with accumulator	4	2–3		
	Immediate with register	5	3–4		
	Immediate with memory	11+EA	3–6		
WAIT	Wait while $\overline{\text{TEST}}$ pin not asserted	3+5n	1	- - - - - - - - -	457
XCHG	Exchange			- - - - - - - - -	60
	Register with accumulator	3	1		
	Register with memory	17+EA	2–4		
	Register with register	4	2		
XLAT/ XLATB	Translate	11	1	- - - - - - - - -	221
XOR	Logical exclusive OR			0 - - - x x u x 0	93
	Register with register	3	2		
	Memory with register	9+EA	2–4		
	Register with memory	16+EA	2–4		
	Immediate with accumulator	4	2–3		
	Immediate with register	4	3–4		
	Immediate with memory	17+EA	3–6		

EA	No. of Clock Cycles
Direct	6
Register indirect	5
Register relative	9
Based indexed (BP)+(DI) or (BX)+(SI) (BP)+(SI) or (BX)+(DI)	7 8
Based indexed relative (BP)+(DI)+DISP or (BX)+(SI)+DISP (BP)+(SI)+DISP or (BX)+(DI)+DISP	11 12

Flag Setting Symbols:

O D I T S Z A P C:
- – Not affected
- x Set or cleared according to the result
- u Undefined
- 0 Cleared to 0
- 1 Set to 1
- r Restored from previously saved value

Conditional Jump Instructions

Instruction	Description	Condition	Aliases	Opposite
JC	Jump if carry	Carry = 1	JB, JNAE	JNC
JNC	Jump if no carry	Carry = 0	JNB, JAE	JC
JZ	Jump if zero	Zero = 1	JE	JNZ
JNZ	Jump if not zero	Zero = 0	JNE	JZ
JS	Jump if sign	Sign = 1	-	JNS
JNS	Jump if no sign	Sign = 0	-	JS
JO	Jump if overflow	Overflow = 1	-	JNO
JNO	Jump if no overflow	Overflow = 0	-	JO
JP	Jump if parity	Parity = 1	JPE	JNP
JPE	Jump if parity even	Parity = 1	JP	JPO
JNP	Jump if no parity	Parity = 0	JPO	JP
JPO	Jump if parity odd	Parity = 0	JNP	JPE

Unsigned Comparisons				
Instruction	Description	Condition	Aliases	Opposite
JA	Jump if above (>)	Carry = 0, Zero = 0	JNBE	JNA
JNBE	Jump if not below nor equal (not <=)	Carry = 0, Zero = 0	JA	JBE
JAE	Jump if above or equal (>=)	Carry = 0	JNC, JNB	JNAE
JNB	Jump if not below (not <)	Carry = 0	JNC, JAE	JB
JB	Jump if below (<)	Carry = 1	JC, JNAE	JNB
JNAE	Jump if not above nor equal (not >=)	Carry = 1	JC, JB	JAE
JBE	Jump if below or equal (<=)	Carry = 1 or Zero = 1	JNA	JNBE
JNA	Jump if not above (not >)	Carry = 1 or Zero = 1	JBE	JA
JE	Jump if equal (=)	Zero = 1	JZ	JNE
JNE	Jump if not equal ()	Zero = 0	JNZ	JE

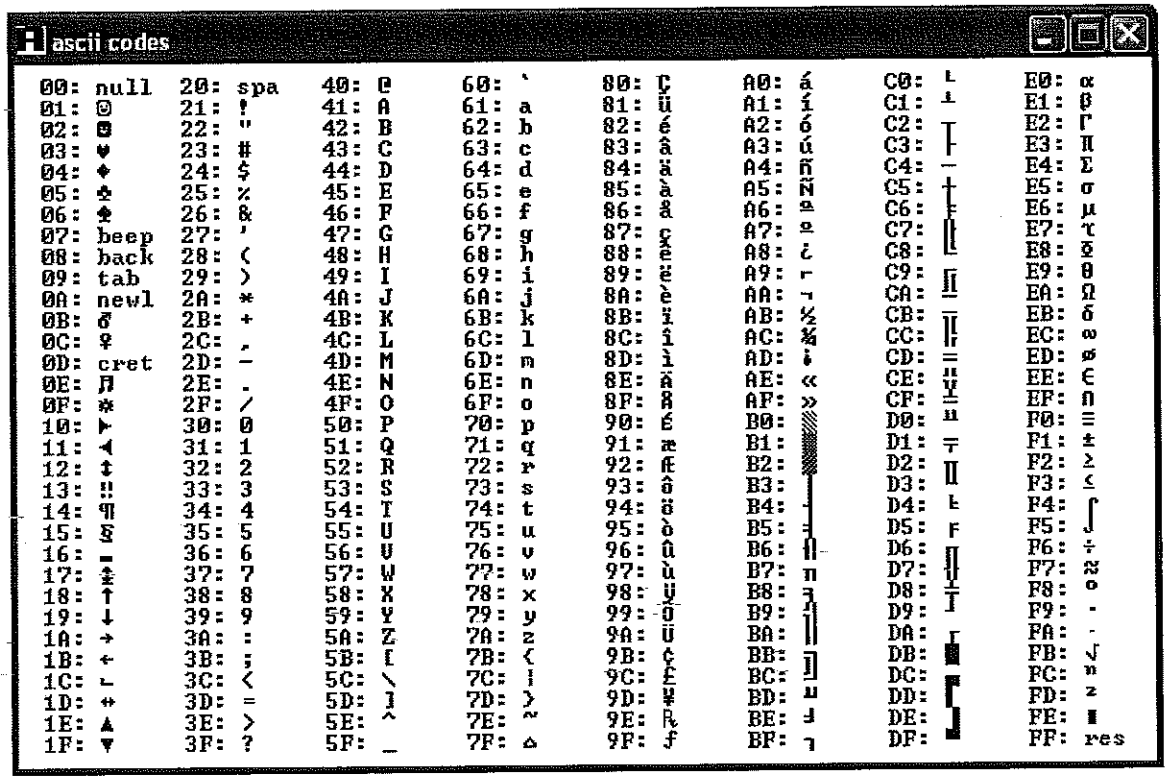
Signed Comparisons				
Instruction	Description	Condition	Aliases	Opposite
JG	Jump if greater (>)	Sign = Overflow & Zero = 0	JNLE	JNG
JNLE	Jump if not less than nor equal (not <=)	Sign = Overflow & Zero = 0	JG	JLE
JGE	Jump if greater than or equal (>=)	Sign = Overflow	JNL	JGE
JNL	Jump if not less than (not <)	Sign = Overflow	JGE	JL
JL	Jump if less than (<)	Sign Overflow	JNGE	JNL
JNGE	Jump if not greater nor equal (not >=)	Sign Overflow	JL	JGE
JLE	Jump if less than or equal (<=)	Sign Overflow or Zero = 1	JNG	JNLE
JNG	Jump if not greater than (not >)	Sign Overflow & Zero = 1	JLE	JG
JE	Jump if equal (=)	Zero = 1	JZ	JNE
JNE	Jump if not equal ()	Zero = 0	JNZ	JE

8086 Flags Register

```
|ODITSZAPC|    Overflow Flag, Direction Flag, Interrupt Flag, Trap Flag,
                Sign Flag, Zero Flag, Auxilary carry Flag, Parity Flag,
                Carry Flag
```

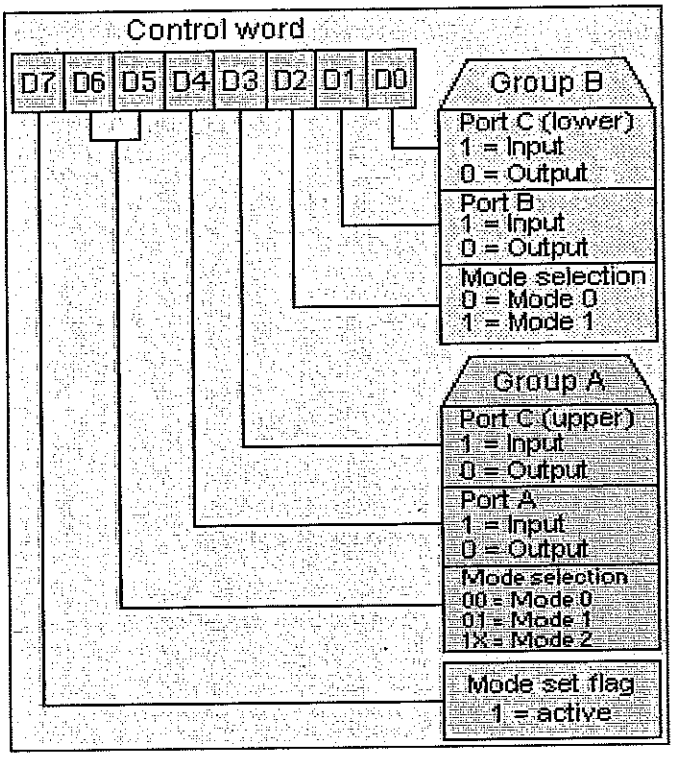
APPENDIX B: ASCII TABLE

ASCII Codes

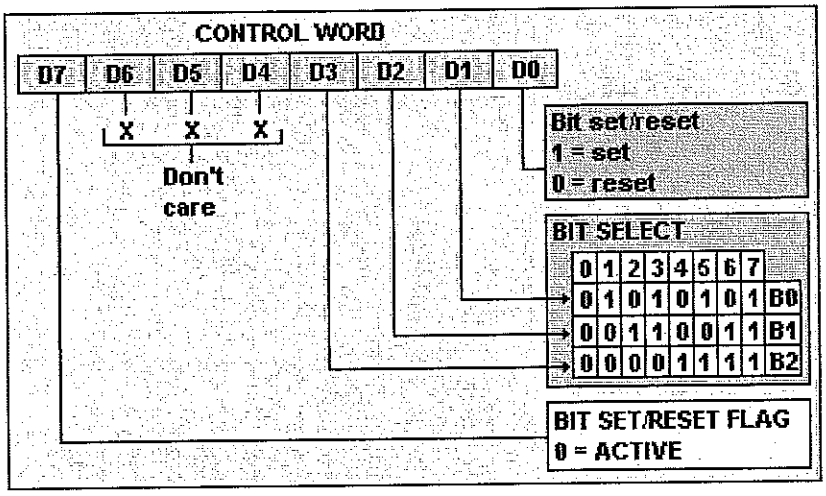


APPENDIX C: 8255 PPI

Control Word



8255 Control Word Format (I/O Mode)



BSR Control Word

APPENDIX D: 8253/8254 PIT

Control Word

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

BCD	Function
0	16-bit binary
1	4-decade BCD

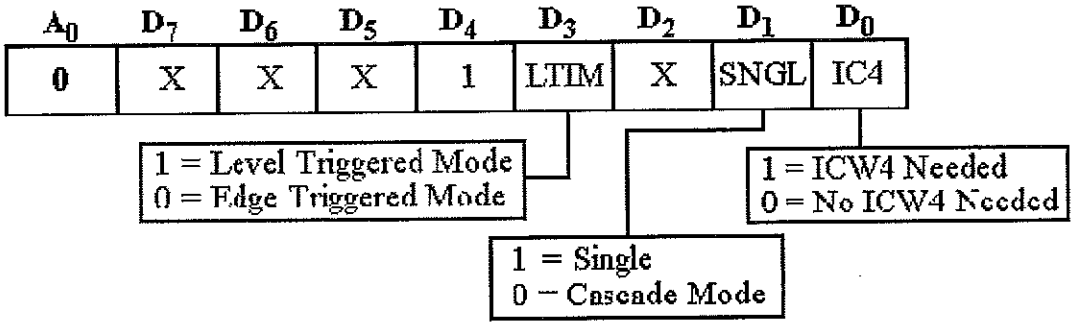
SC1	SC0	Function
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2

RW1	RW0	Function
0	1	R/W LSB only
1	0	R/W MSB only
1	1	R/W LSB then MSB

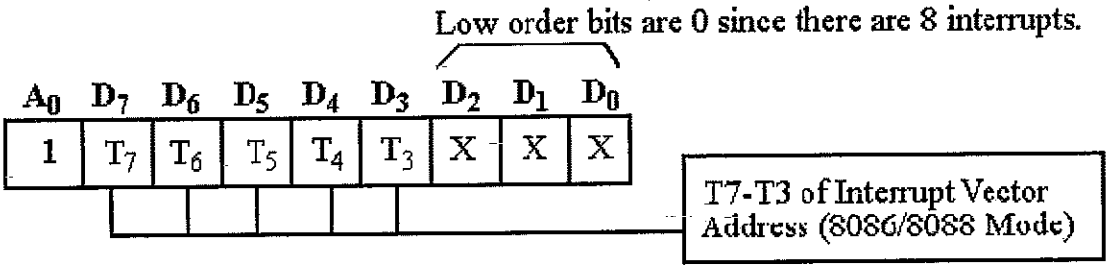
M2	M1	M0	Mode
0	0	0	0
0	0	1	1
X	1	0	2
X	1	1	3
1	0	0	4
1	0	1	5

APPENDIX E: 8259 PIC

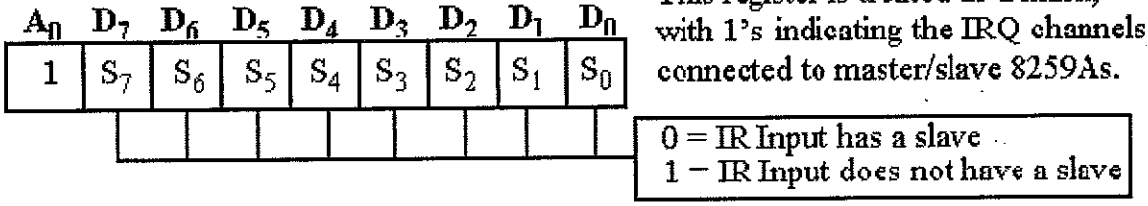
ICW1:



ICW2:



ICW3:



ICW4: