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FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2015**
Programme	:	Diploma in Electrical and Electronic Engineering
Course	:	**EEE2101: Introduction to Digital Electronics**
Date of Examination	:	9th December 2015 (Wednesday)
Time	:	11:00am – 1:00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted :

Nil

Materials provided :

Nil

Examiner(s)	:	**Mr. Steven Khoo Boo Tap**
Moderator	:	Mr. Kevin Tan Geok Su

This paper consists of 11 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: AUG2015 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the letter A through J, respectively, as shown below in Figure 1(a-1). The BCD inputs are labelled as WXYZ, W is the MSB and Z is the LSB. Figure 1(a-2) shows a Common-Anode 7 segment display. Assume all unused inputs as don't care.

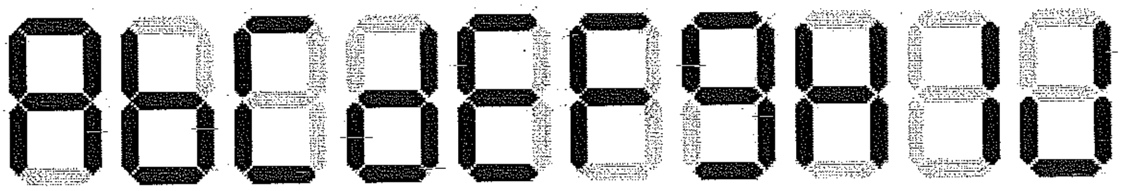


Figure 1(a-1)

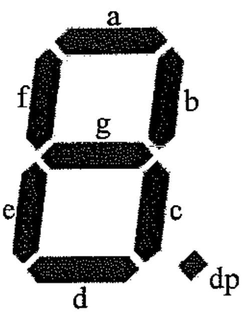


Figure 1(a-2)

(i) Develop the truth table for the inputs to segments a through g of the 7 segment. (4 marks)

(ii) Determine the SOP form of the logic expression for segments b, c and d. (6 marks)

(iii) Implement the logic expression using only 2-input NAND gate with minimum IC consideration. State the number of ICs used. Show all working clearly. (8 marks)

(b) Perform the following number system transformation. Show all workings clearly.

(i) $A4.F4_{16}$ to decimal equivalent with 6 decimal points accuracy.

(3 marks)

(ii) $[10215.01_8 \times 12_8]$ to hexadecimal equivalent with 2 hexadecimal points accuracy.

(4 marks)

Question 2

(a) Figure 2(a) shows the logic symbol of 74HC154 4-bit (1-of-16) decoder with (pin numbers in parentheses). A certain application requires that a 5-bit number be decoded. Use 74HC154 decoders to implement the logic. The binary number is represented by the format $A_4A_3A_2A_1A_0$. Provide details explanation of the fifth bit, A_4 implementation.

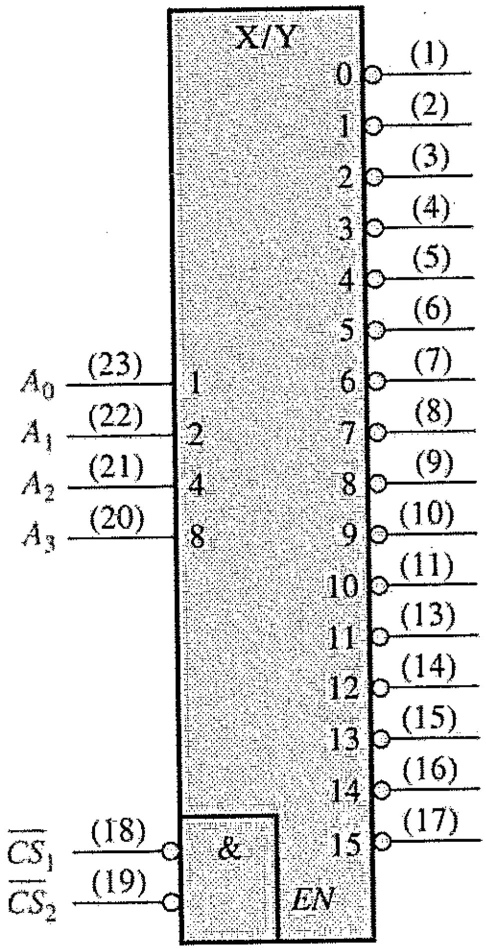


Figure 2(a)

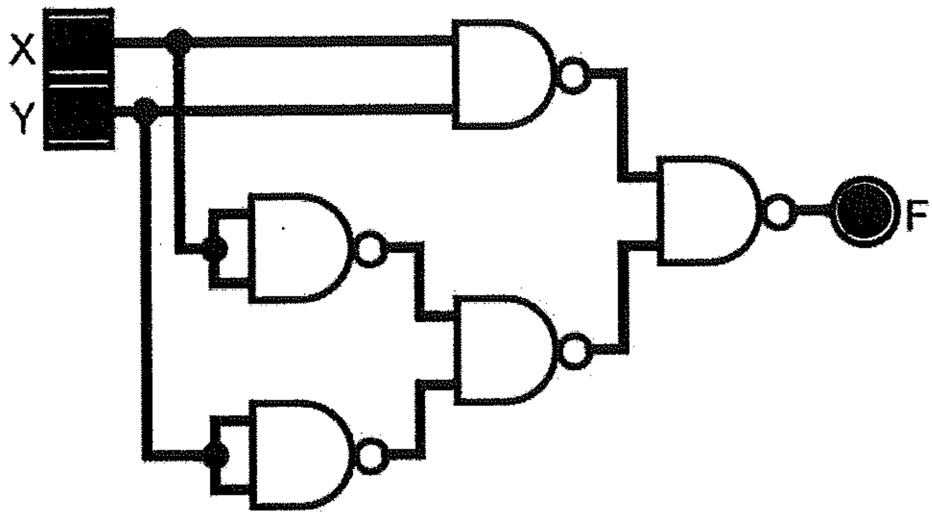
(7 marks)

(b) Using Boolean algebra only, simplify to the simplest SOP form:

(i) $F(A,B,C,D)=\prod(0,1,4,5,6,7)$.

(5 marks)

(ii) $F(X,Y)$



(4 marks)

(c) Use the given Karnaugh map and Boolean algebra to obtain the minimum

(i) SOP expression for the function,
$F(K,L,M,N)=\prod(1,5,7,9,13,15)$.

(3 marks)

(ii) POS expression for the function,
$F(A,B,C,D)=\sum(2,3,8,9,10,12,14,15)$.

(3 marks)

(iii) POS expression for the function,
$F(W,X,Y,Z)=\sum(4,9)+d(10,11,12,13,14,15)$.

(3 marks)

Question 3

(a) Assume that the numbering system used is a 10-bit system. Show all working clearly.

(i) Sketch the range that the numbers can be represented in a two's complement numbering system.

(2 marks)

(ii) Express $[-117_{10} + 258_{10}]$ using two's complement notation.

(4 marks)

(b) Figure 3(b) below shows a 3-bit synchronous counter which is designed so that it performs a special counting sequence. Analyse its operation by determining its counting sequence. Switch S is a control signal used to control the sequence of the counting. Flip-flop FF2 is MSB and FF0 is LSB. Use $D_2T_1D_0$ inputs labelling for Q_2, Q_1 and Q_0 outputs. Show all workings clearly.

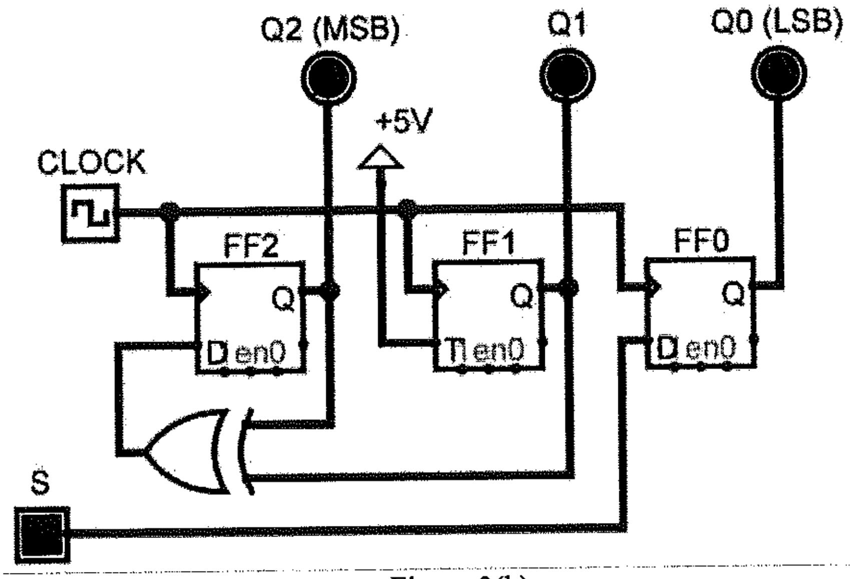


Figure 3(b)

(i) Provide the Boolean expressions from the logic circuit.

(1 mark)

(ii) Provide all Karnaugh maps according to the expressions.

(3 marks)

(iii) Provide the transition table/ next state table with excitation table.

(4 marks)

(iv) Draw the state diagram and comment on the outcome of the states obtained. What application can this circuit be used for?

(4 marks)

(c) Table 3(c) shows the current ratings of TTL series logic gates. A 74AS08 AND gate output is driving **4** Standard TTL gate inputs, **2** Advanced Low-Power Schottky gate inputs and **14** Low-Power Schottky gate inputs. Determine if there is a loading problem.

(4 marks)

TTL Series	Output Drive		Input Loading	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	400μA	16mA	40μA	1.6mA
74S	1.0mA	20mA	50μA	2.0mA
74LS	400μA	8mA	20μA	400μA
74AS	2.0mA	20mA	200μA	2.0mA
74ALS	400μA	8mA	20μA	100μA
74F	1.0mA	20mA	20μA	600μA

Table 3(c)

The 74AS08 AND gate output needs to be used to drive some 74F inputs in addition to the load inputs. How many additional 74F inputs could the output drive without being overloaded?

(3 marks)

Question 4

(a) Design a synchronous 3-bit counter using positive edge-triggered JK flip-flops. Assume all unused states as don't care. The counter will count from 000 ⇨ 111 ⇨ 101 ⇨ 010 ⇨ 000. Use $Q_2Q_1Q_0$ outputs labelling for J_2K_2, J_1K_1 and J_0K_0 inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.

(i) Provide the excitation table used.

(1 mark)

(ii) Provide the transition table/ next state table.

(3 marks)

(iii) Simplify using Karnaugh map and Boolean algebra if necessary.

(3 marks)

(iv) Draw the complete logic circuit diagram with proper label.

(3 marks)

(b) Design a synchronous 3-bit counter that counts in the sequence 101 ⇨ 010 ⇨ 000 ⇨ 111 ⇨ 101. Choose a suitable type of flip flops to use for this design such as D flip flops only or T flip flops only or RS flip flops only. Also, use an appropriate control signal together with flip flops of your choice to load the initial value 101 for the counter using a single reset signal. Assume all unused states as don't care. Use $Q_2Q_1Q_0$ as output labelling. Provide proper labelling for the designed logic circuit. Show all workings clearly.

(i) Provide the excitation table used.

(1 mark)

(ii) Provide the transition table/ next state table.

(3 marks)

(iii) Simplify using Karnaugh map and Boolean algebra if necessary.

(3 marks)

(iv) Draw the complete logic circuit diagram with minimum components consideration.

(4 marks)

(v) Comment and compare with the designed logic circuit in Question 4(a).

(4 marks)

Question 5

(a) Figure 5(a) has three inputs (A, B, C) and two outputs (Y, Z).
Table 5a(i) shows a portion of quadruple 2-input AND gates datasheet.
Table 5a(ii) shows a portion of quadruple 2-input OR gates datasheet.
Table 5a(iii) shows a portion of quadruple 2-input XOR gates datasheet.

(i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly.

(6 marks)

(ii) What is minimum operating frequency that can be applied to this circuit without affecting the functionality of the circuit? State the function of this circuit.

(4 marks)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 15$ pF $R_L = 400\Omega$		27	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table 5a(i) AND gate

Symbol	Parameter	$R_L = 2\ k\Omega$				Units
		$C_L = 15\ pF$		$C_L = 50\ pF$		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 5a(ii) OR gate

Symbol	Parameter	Conditions	$C_L = 15\ pF,\ R_L = 400\Omega$		Units
			Min	Max	
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input LOW		23	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Other Input HIGH		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table 5a(iii) XOR gate

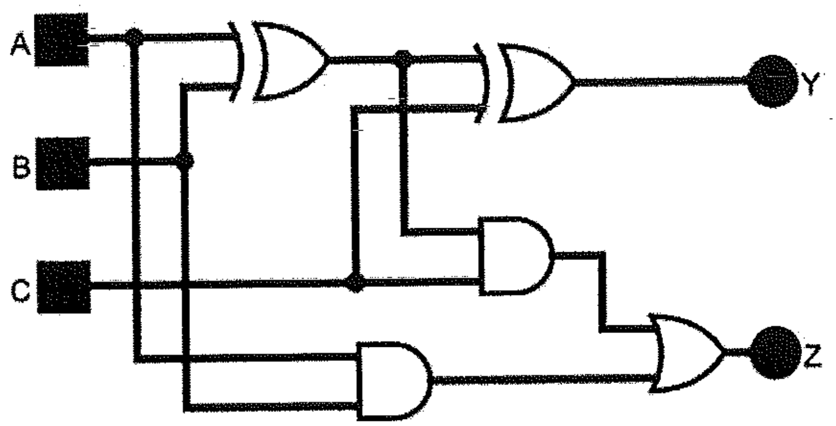


Figure 5(a)

(b) Table 5(b) shows a portion of quadruple 2-input NAND gates (SN74ALS00A) datasheet. Determine the following parameters from this datasheet, show all working clearly:

(i) Fan-out, a gate can safely drive. (3 marks)

(ii) Average Power dissipation, $P_{D(avg)}$ for one gate on a 74ALS00 IC. (3 marks)

(iii) Propagation delay, t_{PD}. (2 marks)

recommended operating conditions

		SN54ALS00A MIN	SN54ALS00A NOM	SN54ALS00A MAX	SN74ALS00A MIN	SN74ALS00A NOM	SN74ALS00A MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8‡ 0.7§			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

‡ Applies over temperature range −55°C to 70°C

§ Applies over temperature range 70°C to 125°C

electrical characteristics over recommended operating free-air temperature range unless otherwise noted

PARAMETER	TEST CONDITIONS		SN54ALS00A MIN	SN54ALS00A TYP†	SN54ALS00A MAX	SN74ALS00A MIN	SN74ALS00A TYP†	SN74ALS00A MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−20		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0		0.5	0.85		0.5	0.85	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.5	3		1.5	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX§ SN54ALS00A MIN	SN54ALS00A MAX	SN74ALS00A MIN	SN74ALS00A MAX	UNIT
t_{PLH}	A or B	Y	3	15	3	11	ns
t_{PHL}	A or B	Y	2	9	2	8	ns

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

Table 5(b)

(c) A binary-weighted-input DAC is shown in Figure 5(c). If the LSB bit resistor has a value of 240kΩ, compute the values of the other input resistors. Also, calculate the V_{out} if the DAC has a binary input of 1011 with Logic 1 (HIGH) as +3.0V and Logic 0 (LOW) as 0V. Assume that R_f equals to 10kΩ. What are the disadvantages of this method of DAC?

(7 marks)

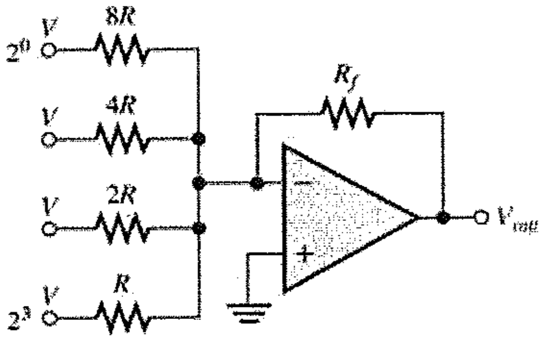


Figure 5(c)

Question 6

(a) A technician uses a logic probe to determine the conditions at the various IC pins as shown in Figure 6(a) and the results are recorded in Table 6(a). Examine these results and determine if the circuit is working properly. If not, identify some of the possible faults as details as possible that can cause this.

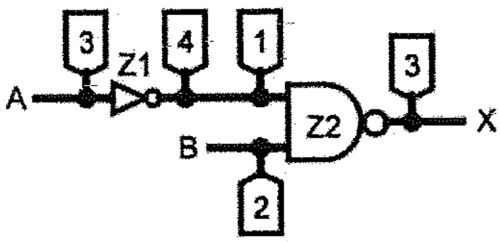


Figure 6(a)

Pin	Condition
Z1-3	Pulsing
Z1-4	LOW
Z2-1	LOW
Z2-2	HIGH
Z2-3	HIGH

Table 6(a)

(6 marks)

(b) The four inputs (W, X, Y, Z) to a communication network system block diagram represent an 8421 code as shown in Figure 6(b). The output (F) is 1 if the decimal number represented by the inputs is exactly divisible by 2. Assume that only valid 8421 codes occur as inputs, other inputs will be treated as 0 for the output. Show all workings clearly.

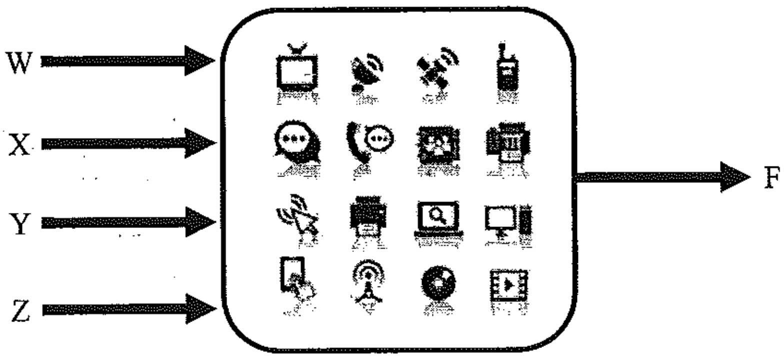


Figure 6(b)

(i) Generate the complete truth-table of the network system.

(3 marks)

(ii) Use Karnaugh map to obtain the simplest expression for the network system.

(3 marks)

(iii) Draw the logic circuit for the network system using only NAND gates with minimum gates and IC consideration. Assume that the complements of the variables are available.

(3 marks)

(iv) Implement the expression obtained in Q6b(ii) using an 8-to-1 MUX with Z as the select line.

(3 marks)

(v) If the company had decided to use only NOR gates for the network design, generate the complete simplest circuit for the network with minimum gates consideration. Assume that the complements of the variables are available.

(3 marks)

(c) A 4-bit R-2R ladder network DAC is shown in Figure 6(c), compute the analog output voltage, V_{out} if the DAC has a binary input of 1011 with Logic 1 (HIGH) as +5.0V and Logic 0 (LOW) as 0V. Assume that R equals to 25kΩ.

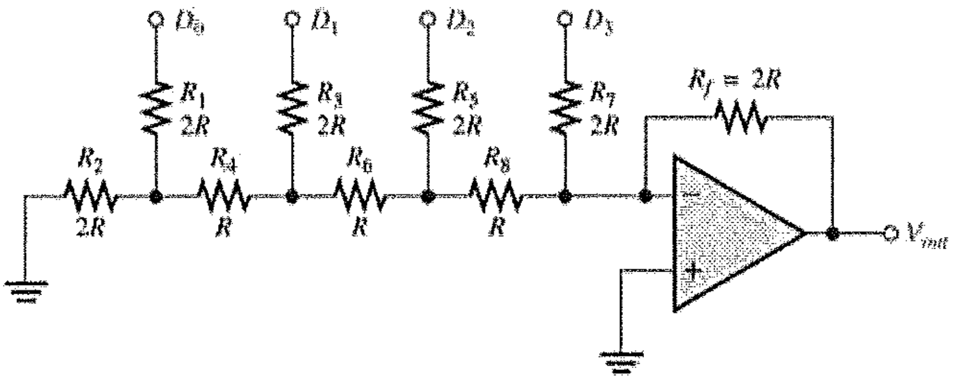


Figure 6(c)

(4 marks)

– THE END –

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