INTI
International College Penang
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FINAL
Examination Paper

(COVER PAGE)

Session	:	**August 2015**
Programme	:	Diploma In Electrical And Electronic Engineering (DEEI)
Course	:	**EEE1106: Analogue Electronics**
Date of Examination	:	7th December 2015 (Monday)
Time	:	5:00pm – 7:00pm
Duration	:	2 Hours Reading Time : Nil
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : **THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL**

Materials Permitted : Non-programmable scientific calculator

Materials Provided : Nil

Examiner(s) : **Mr. Chan Tse Wei**

Moderator : Dr. Khoo Bee Ee

This paper consists of 9 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1106: ANALOGUE ELECTRONICS
FINAL EXAMINATIONS: AUGUST 2015 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin.

Question 1

a. ***"When an amplifier amplifies a voltage signal that it receives, it basically passes this signal to its output port by adding more AC voltages to this signal to increase its amplitude."***

Explain why the above statement is incorrect and give a correct explanation of the amplification process that occurs in an amplifier. [5]

b. An amplifier bandwidth stretches from 200 Hz to 18 kHz.

i. What will happen to the amplifier gain factor at frequency below 200 Hz and above 18 kHz? [2]

ii. What are the root causes of the occurrences described in part (b)(i)? [4]

iii. If the maximum voltage gain of the amplifier at the bandwidth frequencies is 40 dB, what is the output voltage if a 10 mV signal is applied to the amplifier? [4]

c. Figure-Q1(c) shows a common source amplifier circuit. Assume that the load capacitance, C_{load} is sufficiently large that the parasitic capacitances of transistor Q_1 can be ignored.

i. Draw the high frequency small-signal equivalent circuit. [3]

ii. Hence, derive the voltage gain magnitude expression for the amplifier circuit. [5]

iii. If the transistor's transconductance is 2mS and its output resistance is $1.8G\Omega$, $R_D = 2k\Omega$, $R_{signal} = 100\Omega$, and $C_{load} = 2nF$, calculate the voltage gain value at 200 kHz. [2]

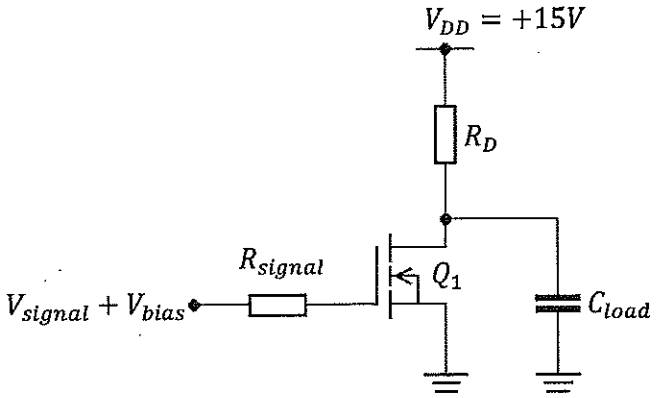

Figure-Q1(c)

Question 2

a. Figure-Q2(a) shows a power amplifier circuit.

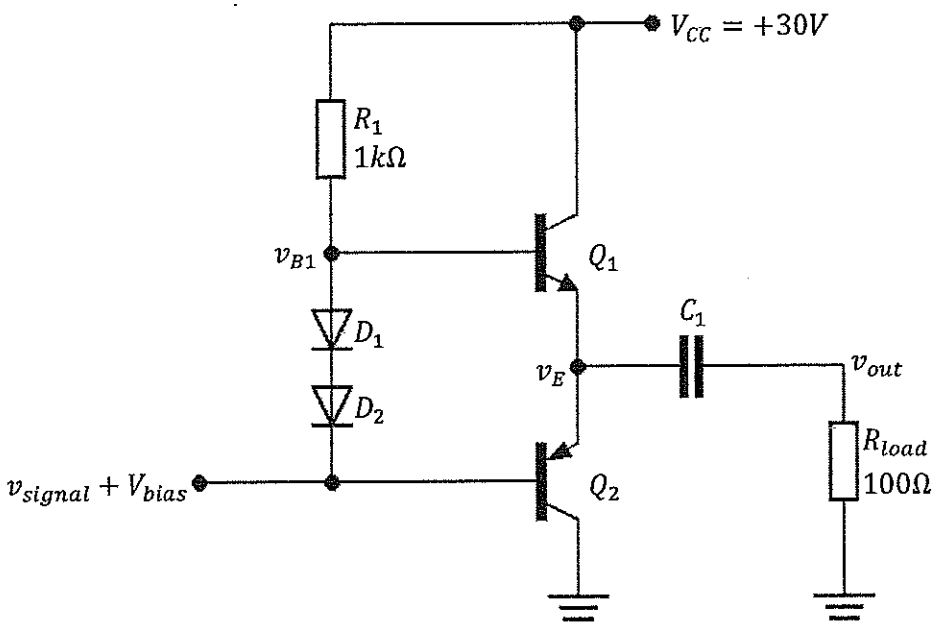

Figure-Q2(a)

i. Identify the name of the power amplifier. [2]

ii. Assume that transistors Q_1 and Q_2 are perfectly matched with their B-E junction barrier voltage being 0.7V. Likewise, D_1 and D_2 are perfectly matched diodes with their forward bias barrier voltage being approximately 0.7V as well. In the absence of v_{signal}, what is the expected voltage at node v_{B1} if V_{bias} is set to 14.3V? [2]

iii. Ideally, what is the expected voltage at node v_E in the absence of v_{signal}? [2]

iv. Ideally, what is the maximum power dissipation in each of the transistor? [4]

v. What is the ideal voltage gain of this power amplifier? [2]

vi. What is the ideal quiescent collector current of this power amplifier? [2]

b. Figure-Q2(b) shows a circuit utilized as a power amplifier. The inset drawing shows the AC model for transistor Q_1.

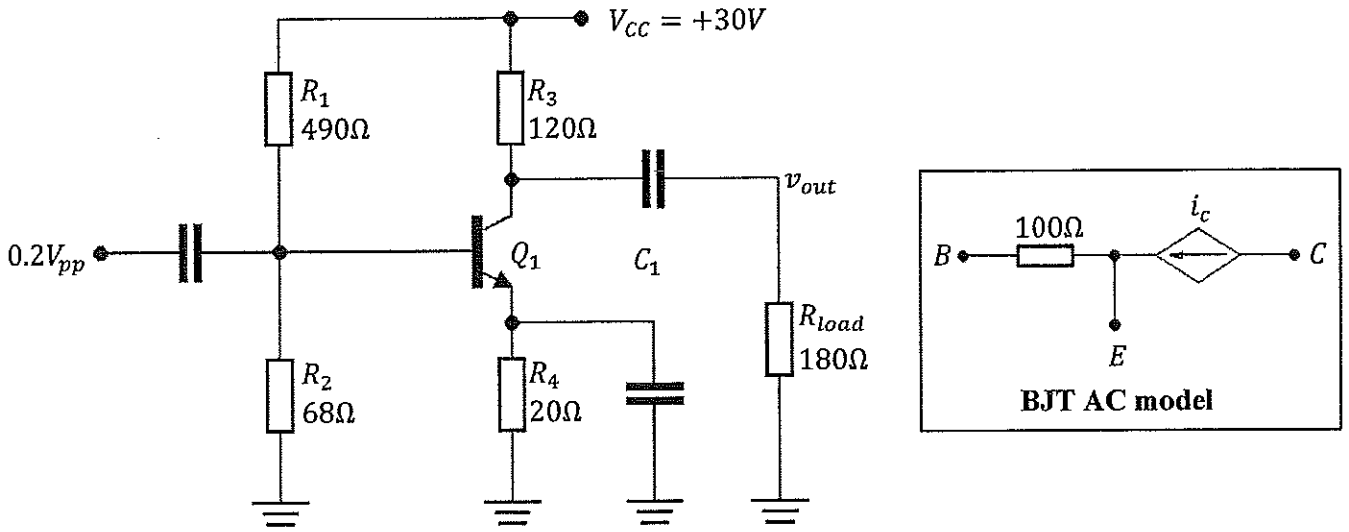

Figure-Q2(b)

i. If the output voltage across resistor R_{load} is 18 V_{pp}, calculate power gain of the amplifier. [4]

ii. Calculate the transistor power dissipation of the amplifier. [4]

iii. Calculate the power efficiency of the amplifier without neglecting any DC current in the circuit. [3]

Question 3

Figure-Q3 shows an op-amp based circuit that is used as a *differential voltage-to-current converter*.

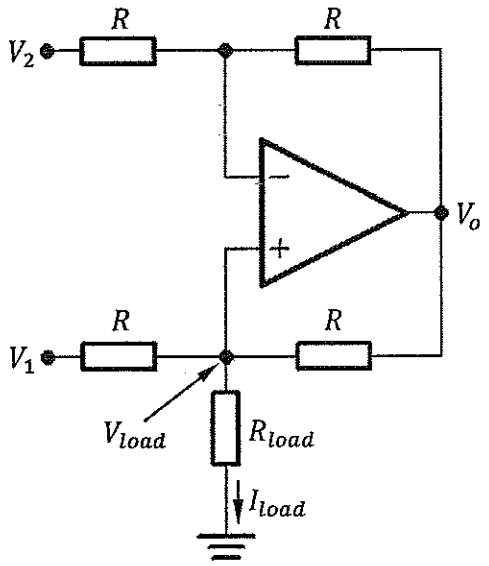

Figure-Q3(a)

a. Derive the nodal equation at the non-inverting input terminal of the op-amp. [3]

b. Derive the nodal equation at the inverting input terminal of the op-amp. [3]

c. Hence show that the current I_{load} is given as,

$$I_{load} = \frac{1}{R}(V_1 - V_2)$$ [4]

d. Base on the findings in part (c), how will the current I_{load} be affected if resistor R_{load} varies within the circuit's operating limits while all other circuit parameters remain unchanged? [2]

e. Assume that $R = 10k\Omega$, $V_1 = 2V$ and $V_2 = 5V$

i. Calculate the current I_{load}. [2]

ii. Comment on the findings in part (e)(i). [2]

f. In order for the voltage-to-current converter to operate as expected, the op-amp must not saturate. For this constraint, show that if the op-amp is powered up with $\pm V_S$ in dual-supply mode operation, then

i. $|V_{load}| < \left|\frac{V_S + V_2}{2}\right|$ [6]

ii. $R_{load} < \left|\frac{V_S + V_2}{V_1 - V_2} \times \frac{R}{2}\right|$ [3]

Question 4

a. In a circuit design scenario, it is desired that a range of signal frequency is to be attenuated while signal frequency lower and higher than this range are to be amplified.

i. State the type of filter that is suitable for implementation in this scenario. [2]

ii. If the order of the filter stated in part (a)(i) is to be second order, express the generic transfer function of this filter. [2]

iii. How can the center frequency of the filter be obtained from the transfer function expression given in part (a)(ii)? [2]

iv. Base on the transfer function expression given in part (a)(ii), quantitatively show that the filter maximum attenuation factor is 0. [4]

b. Figure-Q4(b) shows an active notch filter circuit. All the resistors in the circuit have equal value, R. The same applies to the two capacitors which respectively has capacitance C.

i. Qualitatively determine the output voltage, V_o if V_i = DC voltage. Explain your answer clearly. [3]

ii. Qualitatively determine the output voltage, V_o if V_i = high frequency signal. Explain your answer clearly. [3]

iii. Derive the voltage transfer function of the filter circuit. Hence, determine the Q-factor of this filter circuit. [9]

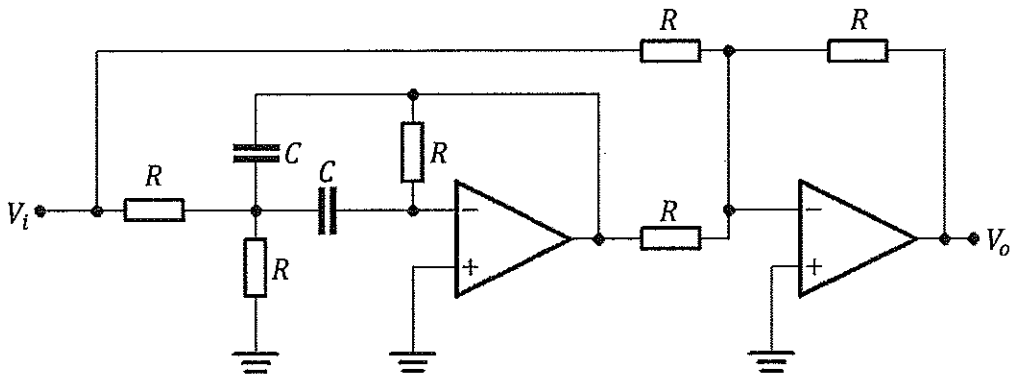

Figure-Q4(b)

Question 5

a. i. The Barkhausen criterion of oscillation states that $A\beta = 1$, where A is the amplifier voltage gain factor, while β is the feedback network transfer function. Explain this equation. [4]

ii. Clearly explain what happen if $A\beta > 1$? [2]

iii. Clearly explain what happen if $A\beta < 1$? [2]

iv. If the feedback network of a harmonic feedback oscillator has a transfer function of $0.03\angle -60°$, base on the Barkhausen criterion of oscillation, what should be the amplifier gain factor? [2]

b. Figure-Q5(b) shows an incomplete schematic diagram of a practical Wien bridge oscillator.

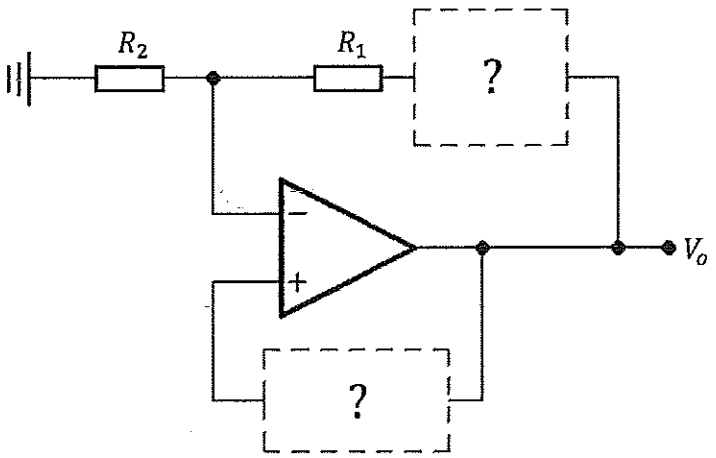

Figure-Q5(b)

i. Complete the schematic diagram in your answer booklet by drawing the remaining circuits in the blocks with the question mark. [4]

ii. When oscillation is sustained, what is the expected phase shift contributed by the feedback network? [1]

c. While experimenting a harmonic oscillator circuit, the followings are concluded:

$$A = j\left(\frac{16 \times 10^6}{\omega}\right)$$

$$\beta = \frac{10^3}{(2 \times 10^3 + j\omega)^2}$$

i. Verify if signal oscillation produced by this oscillator circuit will sustain. [8]

ii. Find the frequency (in Hz) at which the circuit will oscillate. [2]

Question 6

a. i. State two applications of power amplifier. [2]

ii. State three main design considerations for power amplifiers. [3]

iii. Explain why a power amplifier could never achieve 100% efficiency. [2]

iv. Explain the reason for using heatsinks in power amplifier circuits? [2]

v. Explain why crossover distortion occurs in a class B power amplifier. [3]

b. Figure Q6(b) shows a common emitter small signal amplifier circuit. If the BJT transistor has $h_{ie} = 2\ \text{k}\Omega$ and $h_{fe} = 200$, while h_{re} and h_{oe} may be neglected, determine the lower cutoff frequency of the amplifier circuit. [13]

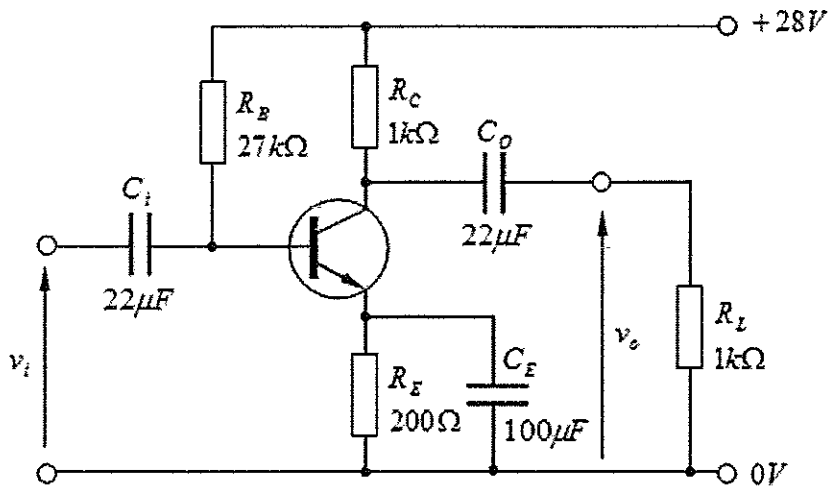

Figure Q6(b)

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