INTI
INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	APRIL 2013
Programme	:	DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING
Course	:	EEE 2101: INTRODUCTION TO DIGITAL ELECTRONICS
Date of Examination	:	29 July 2013
Time	:	5p.m. – 7p.m. Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Examiner(s) : **Khoo Boo Tap**

Moderator : **Shalyn Lim Sheue Hui**

This paper consists of 7 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: APR2013 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) List three advantages of digital data compared to analogue data.

(3 marks)

(b) Express the decimal number +38 and -38 as a 7-bit number in the sign-magnitude, 1's complement and 2's complement form for Table 1(b).

(3 marks)

	+38	-38
Sign-magnitude		
1's complement		
2's complement		

Table 1(b)

(c) Assuming the following binary numbers are in 2's complement system.
i. 01100110
ii. 01110001
Does the sum of the two binary numbers cause an overflow? Explain your answer.

(5 marks)

(d) Perform the following number system transformation. Show all workings clearly.
i) $1001001.10000111011_{BCD}$ to decimal

(2 marks)

ii) 41.6875_{10} to binary

(2 marks)

iii) $CAFE.BABE_{16}$ to octal

(2 marks)

(e) A 24-bit computer utilises the 2's complement signed number scheme.
i) Determine the range of numerical value its 24-bit register holds.

(4 marks)

ii) Describe how the computer performs the subtraction of $28_{10} - 7_{10}$ using 2's complement arithmetic.

(4 marks)

Question 2

(a) Name the three basic logic gates, with their logic symbol and corresponding truth tables.
(5 marks)

(b) Use Boolean algebra to:

i) Express in standard SOP form, $P = AB\bar{C} + \bar{C}D + ABD$

ii) Express in standard POS form, $Q = (A + \bar{B})(\bar{B} + C)(A + \bar{C})$

iii) Simplify, $R = \bar{A}\bar{B}C + ABC + \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C$

iv) Simplify, $S = AB\bar{C} + \overline{A(\bar{B} + \bar{C})(B + C)}$

(12 marks)

(c) A chemical plant needs a microprocessor driven alarm system to warn of critical conditions in one of its chemical tanks. The tank has four HIGH/LOW (I/O) switches that monitor temperature (T), pressure (P), fluid level (L) and weight (W). Design a system that will notify the microprocessor to activate an alarm when any of the following conditions arise:

- High fluid level with high temperature and high pressure
- Low fluid level with high temperature and high weight
- Low fluid level with low temperature and high pressure
- Low fluid level with low weight and high temperature

(8 marks)

Question 3

(a) A full adder is a device that performs binary addition of two single input bits and a carry input bits. It output a sum (S) and a carry output (C_{out}) bit as shown in figure Q3(a) below:

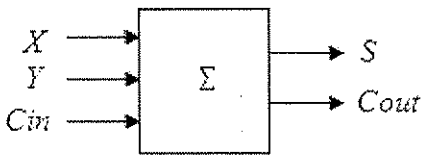

Figure 3(a)

Generate the truth table and hence derive the simplest logic expression of S and C_{out}.
(7 marks)

(b) Using A, B, C_{in} as input and S and C_{out} as output, draw a full adder circuit using two half adders and an OR gate.
(5 marks)

(c) Consider the following combinational logic circuit in Figure 3(c):

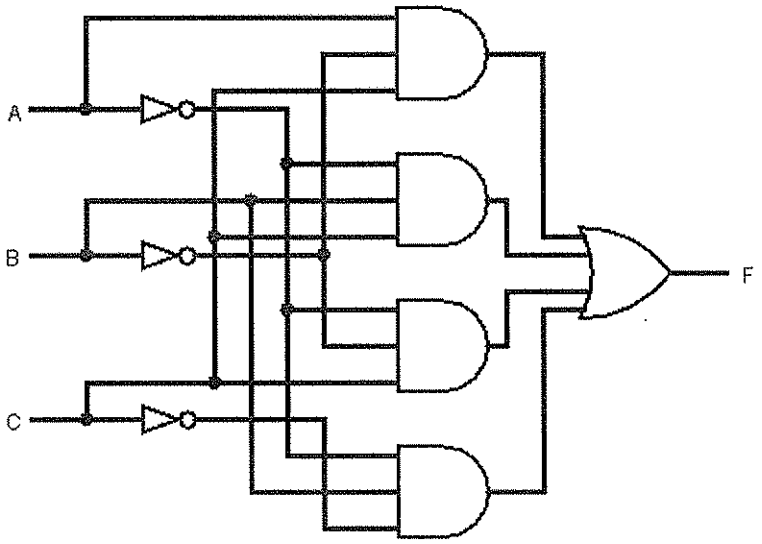

Figure 3(c)

i) Write the Boolean expression for F.

(3 marks)

ii) Assuming the complements of the variables are available, implement the function, F (in its simplest form) using

a) AND-OR logic
b) AND-OR-INVERT logic
c) NAND gates only
d) NOR gates only
e) 8-to-1 multiplexer

(10 marks)

Question 4

(a) For the state diagram shown in Figure 4(a) below, draw the transition table and determine the positive edge-triggered J-K flip-flop control equations before drawing the logic diagram.

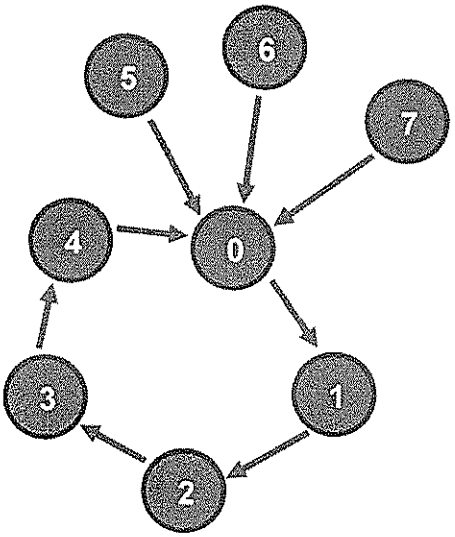

Figure 4(a)

(14 marks)

(b) For the pulse shown in Figure Q4(b) below, graphically determine the following:

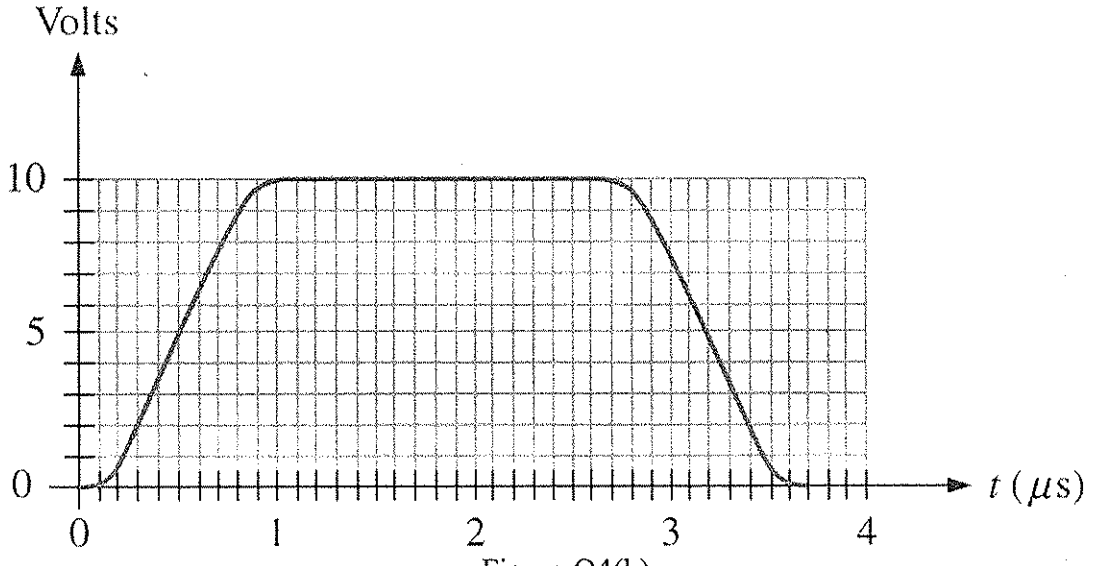

Figure Q4(b)

i) Rise time
ii) Fall time
iii) Pulse time
iv) Amplitude

(4 marks)

(c) Design a circuit comparator that gives a HIGH output if the binary input A_1A_0 is greater than B_1B_0.

(7 marks)

Question 5

(a) i) State the main difference between synchronous and asynchronous counters.

ii) Discuss the advantage and disadvantage of serial transfer over parallel transfer in registers.

(4 marks)

(b) A shift register has eight stages. If the clock frequency is 4MHz, calculate the time needed to load 8 bits of data into the register,

i) in serial

ii) in parallel

(4 marks)

(c) Show the logic diagram of a 4 bit asynchronous count-up counter which uses positive edge-triggered JK flip-flops and has a propagation delay of 8ns. Also determine the total propagation delay and the maximum frequency at which the counter can be operated.

(6 marks)

(d) Given a waveform shown in Figure Q5(d). If the waveform is applied to a sampling circuit and it is sampled every 3ms, determine the following:

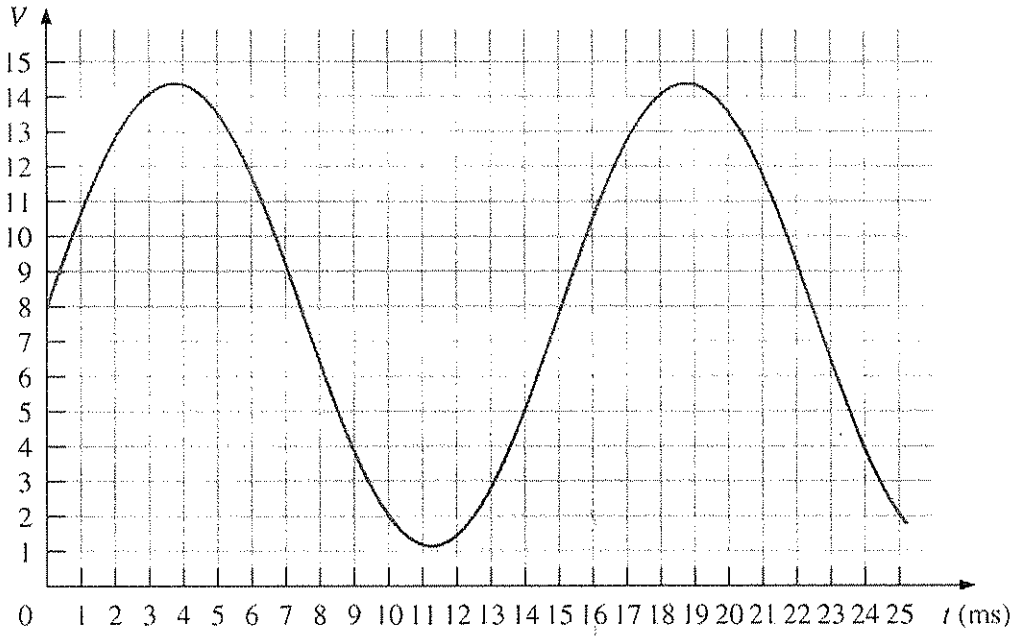

Figure Q5(d)

i) Draw the output of the sampling circuit. Assume a one-to-one voltage correspondence between the input and output.

(4 marks)

ii) If the output in part (i) is applied to a hold circuit, draw the output of the hold circuit.

(4 marks)

iii) If the output in part (ii) is quantized using 4 bits, list the resulting sequence of binary codes.

(3 marks)

Question 6

a) Determine the simplified Boolean expression for the output of the circuit in Figure Q6(a) below. Draw its truth table.

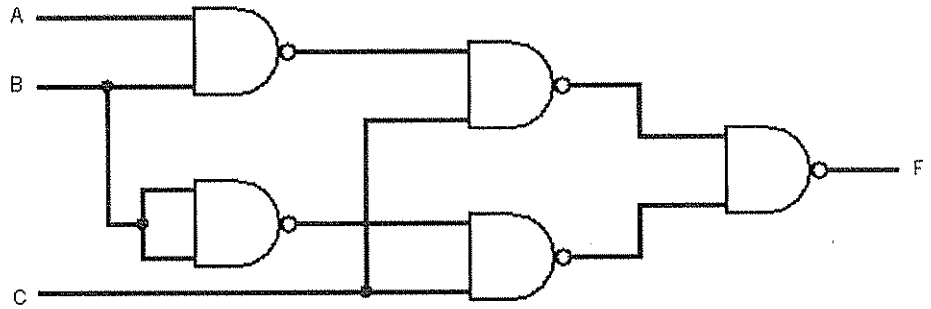

Figure Q6(a)

(5 marks)

b) What is the meaning of the term "integrated" in integrated circuit (IC)? Why it is important in the field of electronics?

(4 marks)

c) Use a Karnaugh map to

i. convert $F = ABC + A\overline{B}CD + \overline{A}B\overline{C}D + ACD$ into its minimum POS form.

(4 marks)

ii. convert $F = (A + B + D)(\overline{A} + \overline{C} + \overline{D})(A + \overline{B} + C)$ into its minimum SOP form.

(4 marks)

iii. minimize $F = A\overline{B} + \overline{C}D + C + \overline{B}\overline{C}D$ in either SOP or POS form.

(4 marks)

d) Draw the circuit of a 4-bit Serial-In-Serial-Out (SISO) shift register using only positive edge-triggered D flip-flops. Label your circuit clearly.

(4 marks)

– THE END –

EEE2101(F)/Apr13/Steven Khoo/23/04/13