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International College Penang

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FINAL
Examination Paper

(COVER PAGE)

Session : APRIL 2013

Programmes : Diploma in Electrical and Electronic Engineering (DEEI)

Course : ELECTRONIC DEVICES AND CIRCUIT THEORY 2 (EEE1103)

Date of Examination : 31 July 2013

Time : 8a.m. – 10a.m. Reading Time: Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Materials permitted : Non-programmable scientific calculator

Materials provided: Semilog Graph Paper (×1)

Examiner(s) : Chan Tse Wei

Moderator : Steven Khoo Boo Tap

This paper consists of 8 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

**EEE1103 : ELECTRONIC DEVICES AND CIRCUIT THEORY 2
FINAL EXAMINATION : APRIL 2013 SESSION**

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin.

Question 1

- a. i. Differentiate the operation of transistors used in class-A and class-B power amplifiers in terms of their respective conduction angle. [2]
- ii. Why power amplifiers will not be 100% efficient practically? [2]
- iii. Draw the basic circuit configuration of a complementary pair push-pull class-B power amplifier. Briefly explain the major problem faced by this type of amplifier. [5]
- iv. Determine the maximum collector power dissipation for one transistor, if the complementary pair push-pull class-B power amplifier is powered by 20V and is delivering power to a 40Ω load. [3]
- v. Determine the maximum output power of the power amplifier described in part (a)(iv). [3]
- b. i. Assume ideal operation and perfectly matched components, determine the quiescent voltage at the input node of the power amplifier circuit in Figure-Q1(b). [2]
- ii. Determine the minimum power rating most suited for resistors R_1 and R_2 . [3]
- iii. If V_m is a sinusoidal waveform of 1V peak and 1kHz, sketch the voltage waveform at the base of transistors T_1 and T_2 respectively, label the voltage levels clearly. [3]
- iv. With the same V_m described in part (b)(iii), determine the AC power delivered to the 8Ω load. [2]

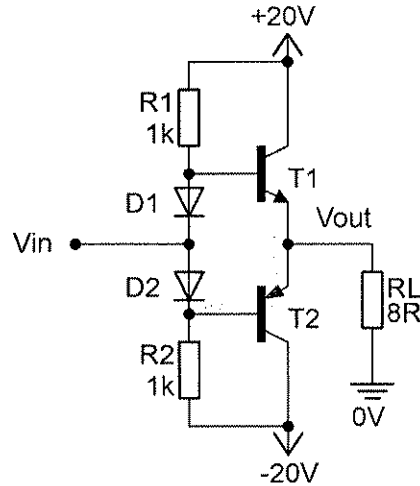


Figure-Q1(b)

Question 2

a. Table-Q2(a) shows a list of experiment results conducted on a voltage amplifier.

f (kHz)	0.01	0.05	0.1	0.5	1	5	10
$A_v = v_o / v_i$	20	20	20	19.98	19.90	17.89	14.14

f (kHz)	20	30	40	50	100	500	1000
$A_v = v_o / v_i$	8.94	6.32	4.85	3.92	1.99	0.40	0.2

Table-Q2(a)

- i. Draw the frequency response ($A_{v(dB)}$ vs f) of the voltage amplifier on the semilog graph paper provided. [8]
- ii. Approximate the bandwidth of the voltage amplifier. [2]
- iii. Approximate the unity gain frequency of the voltage amplifier. [1]
- iv. Determine the roll-off rate of the amplifier at high frequency band. [2]

- b. i. Draw the AC equivalent circuit for the amplifier shown in Figure-Q2(b). Transistor T_1 has $g_m = 2\text{mS}$ and $r_d = 100\text{k}\Omega$. Ignore all parasitic and wiring capacitances in the circuit. [3]
- ii. Determine the cutoff frequency contributed by capacitor C_1 . [2]
- iii. Determine the cutoff frequency contributed by capacitor C_2 . [6]
- iv. Determine the cutoff frequency of the amplifier. [1]

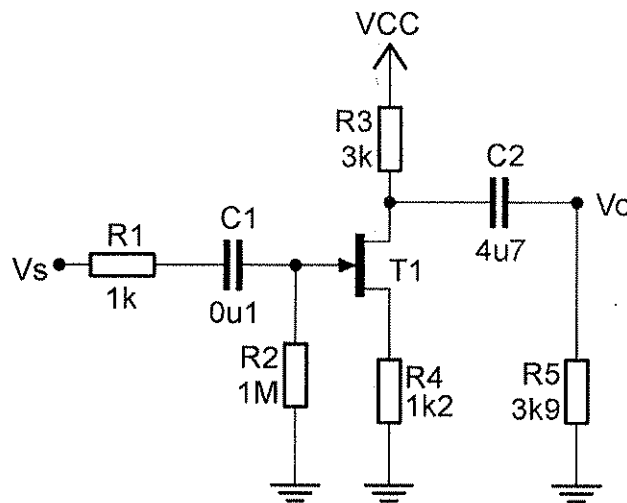


Figure-Q2(b)

Question 3

- a. Draw the operational amplifier (op-amp) circuit model which comprise of an input resistance, an output resistance and a voltage dependent voltage source. [3]
- b. Draw the schematic diagram of the following op-amp based circuits:
- Inverting amplifier [3]
 - Integrator [3]
 - Differential amplifier [3]
 - Non-inverting Schmitt triggered comparator [3]

- c. i. Assume ideal op-amp operation, show that the circuit in Figure-Q3(c) is a voltage dependent current source where $I_{out} = kV_{in}$. Determine the expression of k in terms of the circuit's resistance(s). [5]
- ii. If the op-amp is powered by $\pm 18V$ and V_{in} is fixed at $5V$, determine the limiting value of R_L for the circuit in Figure-Q3(c) to remain operating as a voltage dependent current source. [5]

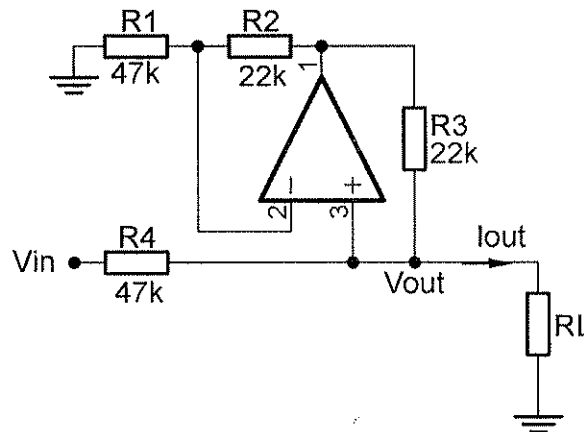


Figure-Q3(c)

Question 4

- a. One useful application of operational amplifier (op-amp) is to build active filter circuits.
- What is an active filter circuit? [3]
 - What is the purpose of the op-amp in an active filter circuit? [3]
 - State four common types of active filter circuits. [2]
 - Draw the ideal frequency response of each type of active filter circuit stated in part (a)(iii). [4]
 - State the generic transfer function expression (in s-domain) of each type of active filter circuit stated in part (a)(iii). [4]

- b. i. Derive the voltage transfer function, $V_{out}(s)/V_{in}(s)$, of the circuit in Figure-Q4(b) in terms of C and R . [5]
- ii. Identify, either quantitatively or qualitatively, the type of filter implemented by the circuit in Figure-Q4(b). [2]
- iii. Suggest a method to reduce the bandwidth of the circuit. [2]

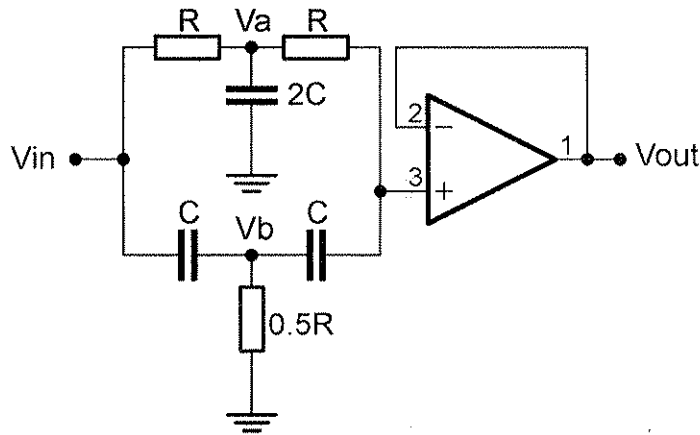


Figure-Q4(b)

Question 5

- a. i. Draw the schematic diagram of a basic Wien bridge oscillator circuit. [3]
- ii. Determine the oscillation frequency if the feedback network has equal-valued capacitance of 330pF and equal-valued resistance of $47\text{k}\Omega$. [3]
- iii. If the feedback factor of the Wien bridge oscillator is 0.5 at the oscillation frequency, what should be the amplifier gain value so that oscillation is sustained? [3]
- b. i. Show how a Schmitt trigger comparator and an integrator can be connected to form a relaxation oscillator. [3]
- ii. If all the resistors used in the relaxation oscillator described in part (b)(i) are $10\text{k}\Omega$ and the capacitor used is 470nF , determine the frequency of the square wave being produced by this oscillator circuit. [3]

- c. Figure-Q5(c) shows an RC phase-shift oscillator circuit.
- i. Write node equations for node- V_1 , node- V_2 and node- V_3 respectively. Simplify each equation as much as possible. [6]
 - ii. Making use of the node equations derived in part (c)(i), show that the circuit in Figure-Q5(c) generates a frequency given by $f_o = \frac{0.082}{CR}$. [4]

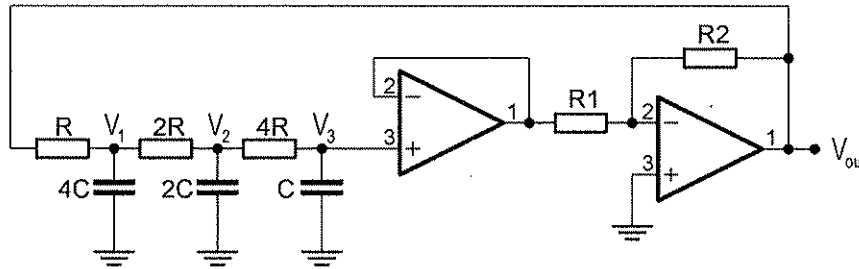


Figure-Q5(c)

Question 6

- a.
 - i. What is voltage regulation? [2]
 - ii. List the two common types of linear voltage regulator. [2]
 - iii. How does one differentiate the types of linear voltage regulator listed in part (a)(ii)? [6]
 - iv. A voltage regulator produces 5V when unloaded. However, its output voltage drops to 4.85V when maximum current is drawn from this regulator. Determine the regulation of this voltage regulator in percentage. [3]

- b. Figure-Q6(b) shows a simple voltage regulator utilizing the zener diode. The zener diode is rated at 5V and has a dynamic resistance of 50Ω , that is in the reverse bias condition, the zener diode can be modeled as a 5V source in series with a 50Ω resistor. The input voltage is modeled as 20V DC source in series with a 2V peak-to-peak AC ripple source.
 - i. Determine the quiescent current through the zener diode. [2]
 - ii. Draw the AC equivalent circuit model for the regulator circuit. [3]

- iii. Use the AC equivalent circuit model drawn in part (b)(ii) to determine the peak-to-peak ripple component of the output voltage. [3]
- iv. If a 100Ω load is connected across the output terminal, how does it affect the quiescent output voltage? [4]

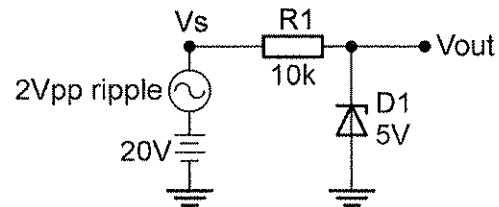


Figure-Q6(b)

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Student Name: _____

Student Identification: _____

