INTI
INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	April 2013
Programme	:	DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEI)
Course	:	**EEE1102 : ELECTRONIC DEVICES AND CIRCUIT THEORY I**
Date of Examination	:	31 July 2013
Time	:	8a.m. – 10a.m. Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Materials permitted :

Non Programmable Scientific Calculator

Materials provided :

Nil

Examiner(s) : **Liong Han Wen**

Moderator : **Chan Tse Wei**

This paper consists of 7 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

EEE 1102: ELECTRONIC DEVICES AND CIRCUIT THEORY 1
FINAL EXAMINATION: APRIL 2013 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in brackets at the right-hand margin.

Question 1

a. For Figure Q1(a), calculate V_{OUT} and current flow through the diode D1. Assume all the diodes are practical model. (8 marks)

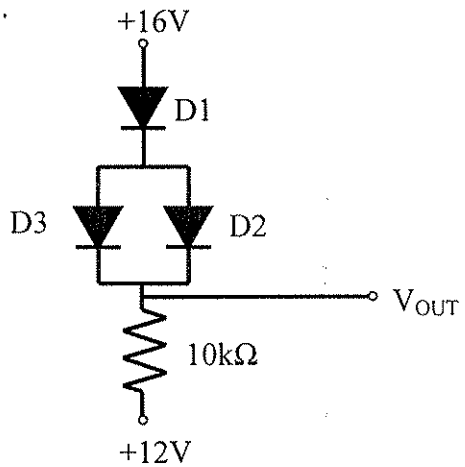


Figure Q1(a)

b. Sketch the output waveform(V_{OUT}) of the following rectifier circuits. The input waveform is shown in Figure Q1(b). Assume all the diodes in this part are ideal.

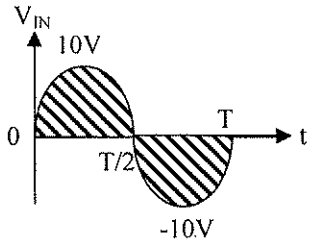
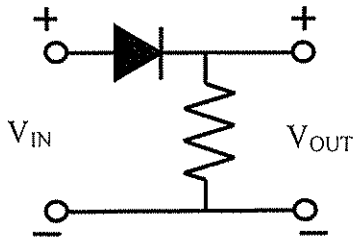
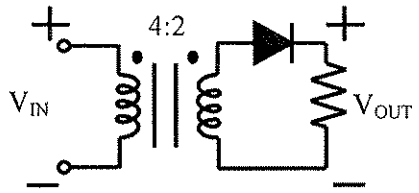


Figure Q1(b)

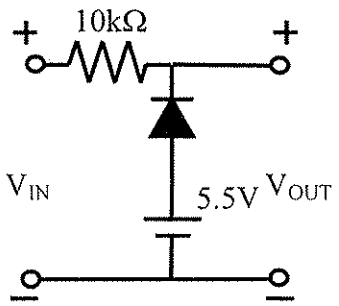
i. (3 marks)



ii. (5 marks)



iii. (5 marks)



c. An NPN transistor is to be operated at a collector current of 50mA. How high can V_{CE} be without exceeding a maximum power of 1.2W? (4 marks)

Question 2

a. For the input waveform shown in Figure Q2(a), design a clipper circuit to produce the resulting output. Use practical silicon diodes for your design. (10 marks)

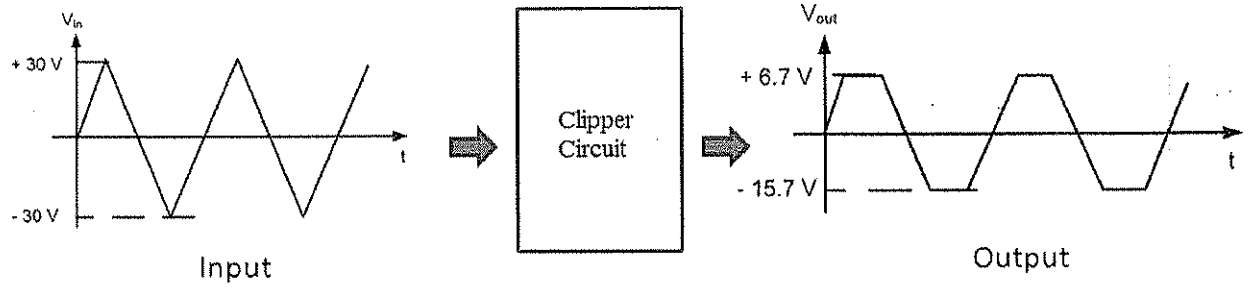


Figure Q2(a)

b. When a 60Hz sinusoidal voltage is applied to the input of a full-wave rectifier, what is the output frequency? (3 marks)

c. For the transistor circuit in Figure Q2(c),

i. What is V_{CE} when $V_{IN} = 0V$? (2 marks)

ii. What is the required minimum value of I_B is required to saturate this transistor if β_{DC} is 250? (5 marks)

iii. Calculate the maximum value of R_B when $V_{IN} = 5V$ and the transistor is just saturated. (5 marks)

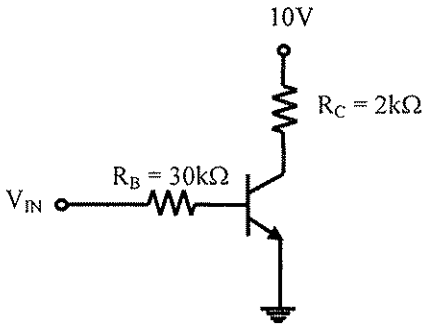


Figure Q2(c)

Question 3

a. A student attempts to build a circuit that will turn a DC motor(Mtr) on and off with a pushbutton as shown in Figure Q3(a). Unfortunately, there is something wrong with the circuit, because the motor does not turn on no matter what is done with the switch. Correct the error(s) in this circuit, showing how it must be set up so that the transistor functions as intended. (5 marks)

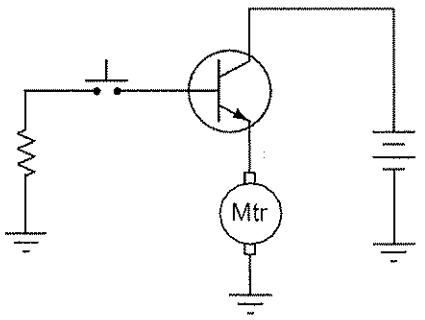


Figure Q3(a)

b. Determine the minimum input voltage (Vin) required for regulation to be established in Figure Q3(b). Assume an ideal zener diode with $I_{ZK} = 1.5mA$ and $V_Z = 14V$. (4 marks)

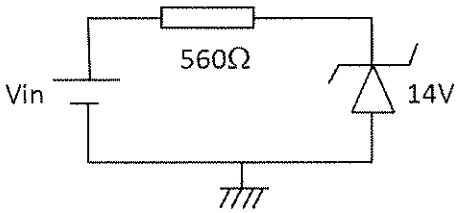


Figure Q3(b)

c. The base bias circuit in Figure Q3(c) is subjected to a temperature variation from 0°C to 70°C. The β_{DC} decrease by 50 percent at 0°C and increase by 75 percent at 70°C from its nominal value of 110 at 25°C. What is the % of changes in I_C? (10 marks)

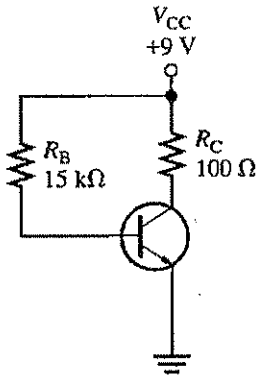


Figure Q3(c)

d. Sketch a collector characteristic curve of a typical bipolar junction transistor. Identify the different regions of the curve. (6 marks)

Question 4

a. Figure 4(a) is a multistage amplifier and the second stage is loaded with a load resistor, R_L of 18kΩ. Given R_1=R_5=33kΩ, R_2=R_6=8.2kΩ, R_3=R_7=3.3kΩ, R_4=R_8=1kΩ and βac=β_{DC}=170. Determine

i. The voltage gain for each stage. (15 marks)

ii. Overall voltage gain. (3 marks)

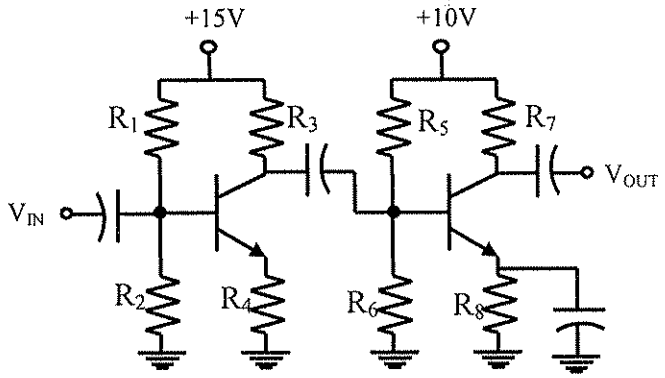


Figure Q4(a)

b. Sketch the construction of Depletion MOSFET(both p and n channel). State one difference between the operation of D-MOSFET and E-MOSFET. (7 marks)

Question 5

a. A load resistance(R_L) is capacitively coupled to the emitter in Figure Q5(a). What value of R_L will cause the voltage gain become 0.8? (13 marks)

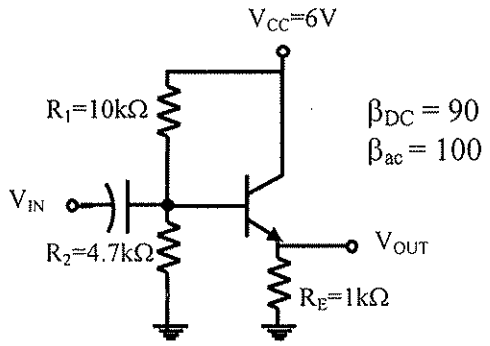


Figure Q5(a)

b. Determine the value of Rs required for a self-biased n-channel JFET that has the transfer characteristic curve shown in Figure Q5(b). (6 marks)

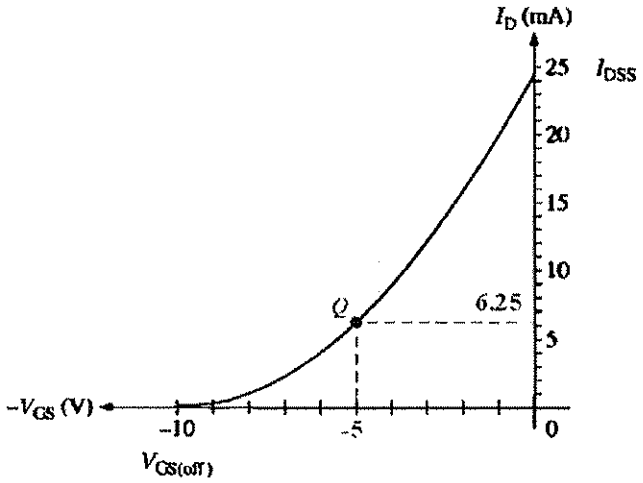


Figure Q5(b)

c. Determine each branch current (I_{BQ},I_{EQ} and I_{CQ}) in Figure Q5(c). What is the value of β_{DC}? (6 marks)

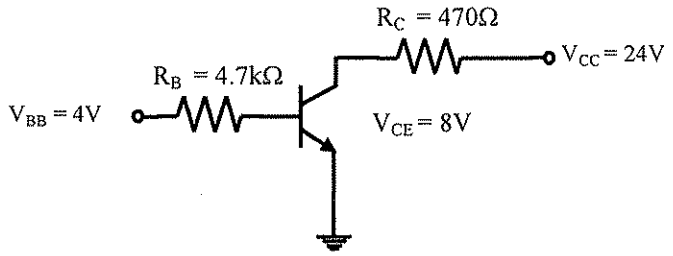


Figure Q5(c)

Question 6

a. Determine the values of Rc, R_E and R_2 for the circuit of Figure Q6(a) with the operating point indicated. Given $V_E=0.1V_{cc}$ and $R_1 = 10k\Omega$. (16 marks)

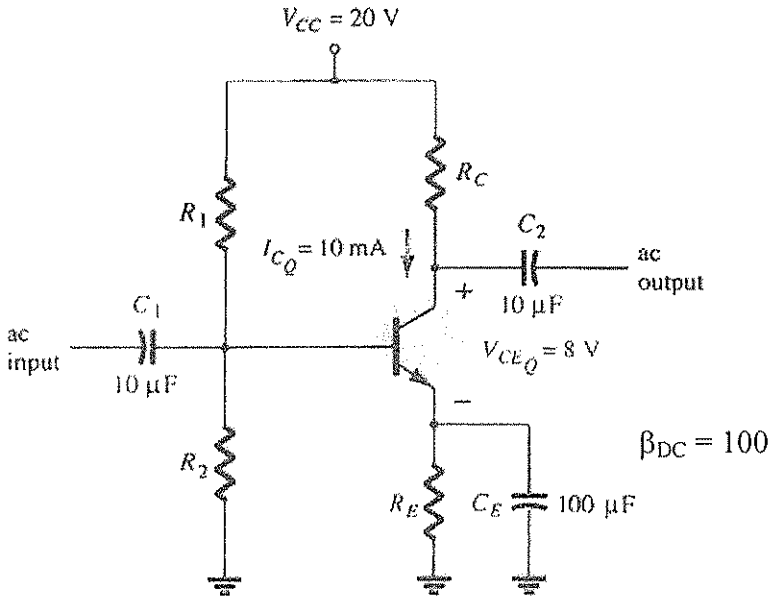


Figure Q6(a)

b. What is the total ac output voltage of the unloaded amplifier shown in Figure Q6(b). Given I_D = 1.96mA. For this particular JFET, I_{DSS} is 12mA and $V_{GS(off)}$ is -3V. (9 marks)

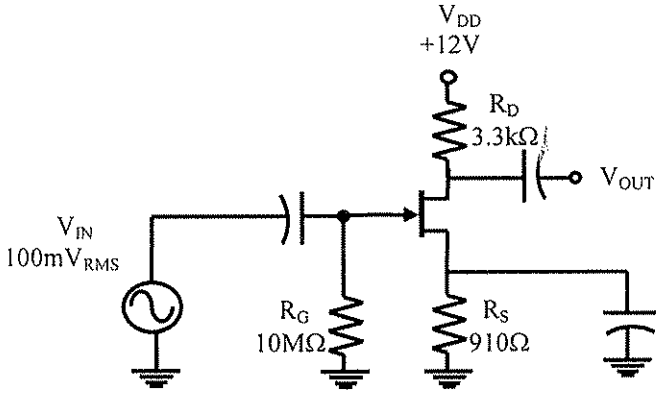


Figure Q6(b)

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