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FINAL
Examination Paper

(COVER PAGE)

Session : AUGUST 2012

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : **EEE2101 : INTRODUCTION TO DIGITAL ELECTRONICS**

Date of Examination :

Time : Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet Provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Materials permitted : Non-programmable scientific calculator

Materials provided : **Appendix-1 and Appendix-2**

Examiner(s) : **Chan Tse Wei**

Moderator :

This paper consists of 7 printed pages, including the cover page.

Question 2

a. A 2-input logic gate is applied with signals A and B simultaneously. The timing diagram of the input signals are shown in Figure-Q2(a) respectively.

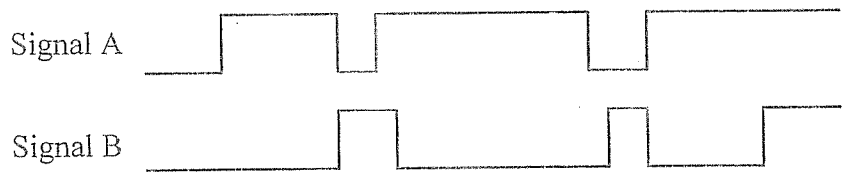


Figure-Q2(a)

Draw the timing diagram (in Appendix-1) of the output signal for each of the following logic gate implementation.

i. AND gate [4]

ii. NOR gate [4]

iii. XOR gate [4]

Note: Attached Appendix-1 to your answer booklet.

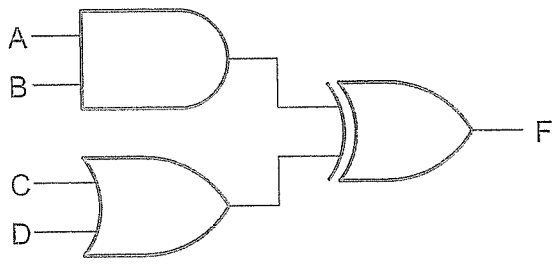


Figure-Q2(b)

b. i. Express the Boolean function of output F in sum-of-product form. [3]

ii. Express the Boolean function of output F in product-of-sum form. [4]

iii. Redraw the circuit using NAND gates only so that an active low output is implemented. [3]

c. Show that $AB + \overline{A}C + BC = AB + \overline{A}C$ [3]

Question 4

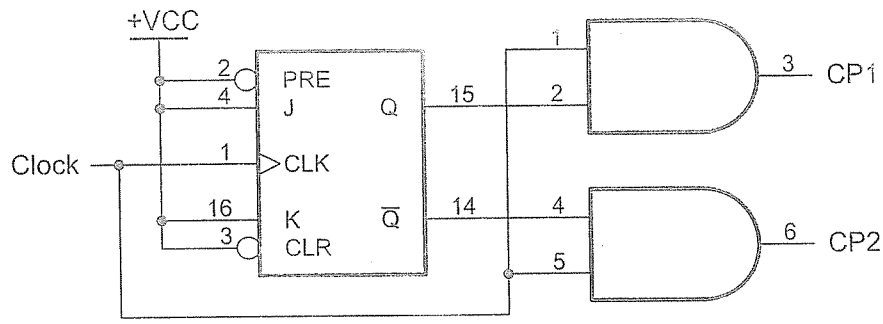


Figure-Q4(a)

a. i. State the mode of operation of the JK flip-flop in Figure-Q4(a). [2]

ii. Draw the timing diagram for CP1 and CP2 respectively in respond to a clock signal shown in Appendix-2.

Note: Attach Appendix-2 to your answer booklet. [6]

iii. State the application of the circuit in Figure-Q4(a). [2]

b. A MOD-5 synchronous up counter is needed for a digital system.

i. Draw a state diagram for the required counter; all unused states which occur will reset the counter on the next clock pulse to zero state. [2]

ii. Produce a transition table for the counter. [4]

iii. If JK flip-flops are to be used in the design of the counter, derive the simplest excitation expression for each flip-flop input. [9]

Question 6

a. An 8-bit DAC produces an output current in proportion to its digital input. For a digital input of 00010100, an output current of 10mA is produced.

i. What will the output current be if the digital input is 00011101? [3]

ii. What is the maximum output current produced by this DAC? [3]

iii. What should the digital input be if a 100mA output current is required? [3]

b. Assume that the 8-bit DAC described in part 6(a) uses a –5V to represent a digital input 1 while a 0V to represent digital input 0, and the load resistance is 130Ω.

i. Draw an $R/2^nR$ DAC that will implement the DAC described to supply current to the 130Ω load resistor. [3]

ii. Suggest all the resistances required in the DAC. [8]

iii. State the main shortcoming of this type of DAC. [2]

c. Suggest an alternative DAC that will resolve the shortcoming of the DAC stated in part 6(b)(iii). Draw the schematic diagram of the suggested DAC. [3]

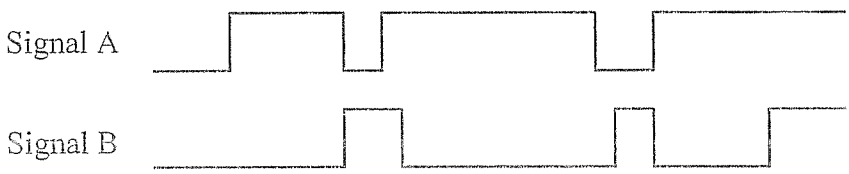
– THE END –

Appendix 1

Student Name:	
Student ID:	

Question 2

a.



i. AND gate: .....

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ii. NOR gate: .....

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iii. XOR gate: .....

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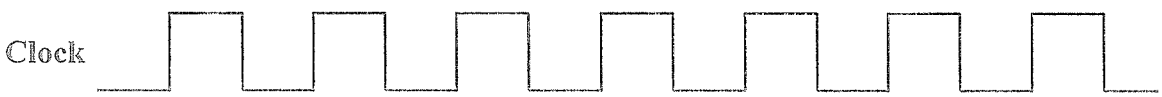
Appendix 2

Student Name:	
Student ID:	

Question 4(a)(ii)



Q

Q'

CP1

CP2