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FINAL
Examination Paper

(COVER PAGE)

Session : AUGUST 2012

Programmes : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE1103 : ELECTRONIC DEVICES AND CIRCUIT THEORY 2

Date of Examination : 12 December 2012

Time : 5p.m. – 7p.m. Reading Time: Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove this question paper from the examination venue.

Materials permitted : Non-programmable scientific calculator

Materials provided: NIL

Examiner(s) : Chan Tse Wei

Moderator : Ooi Beng Lee

This paper consists of 9 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

EEE1103 : ELECTRONIC DEVICES AND CIRCUIT THEORY 2
FINAL EXAMINATION : AUGUST 2012 SESSION

Instructions: This paper consists of SIX (6) questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin.

Question 1

a. Even though class A power amplifier is not the most efficient way to operate a transistor, but it is still a popular way for such application. Why is that so? [3]

b. Figure-Q1(b) shows a voltage divider bias class B/AB power amplifier.

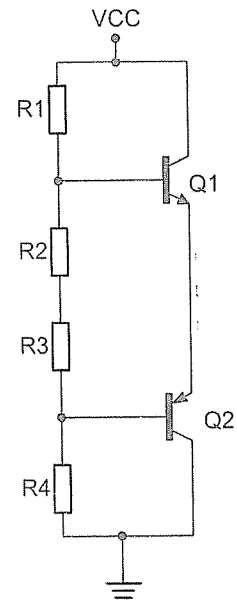

Figure-Q1(b)

i. The transistors in Figure-Q1(b) are complementary. What does that mean? [3]

ii. What is the basic requirement for resistors R1, R2, R3 and R4? [4]

iii. If the V_{BE} of transistors Q1 and Q2 are 0.7V, what is the total voltage drop across resistor R2 and R3? [2]

iv. The configuration in Figure-Q1(b) reduces crossover distortion but the ultimate danger is thermal runaway. Why is that so? [3]

c. Figure-Q1(c) shows a diode bias class B/AB power amplifier.

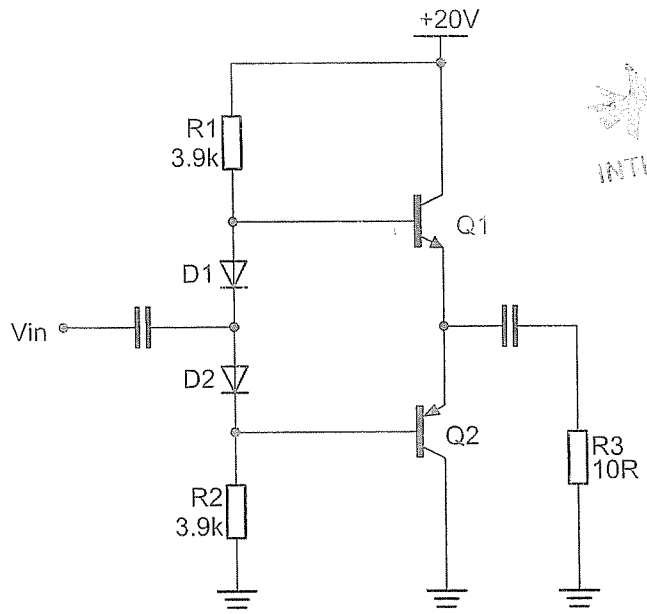

Figure-Q1(c)

i. Assuming that V_{in} = 0V, the forward bias voltage for D1 and D2 is 0.7V respectively and they match the B-E junctions of transistor Q1 and Q2. Also, the quiescent base currents of transistors Q1 and Q2 are negligible. Calculate the amount of DC current drawn from the 20V DC supply. [3]

ii. What are the quiescent voltage values at the base of transistor Q1 and Q2 respectively? [4]

iii. Assume that transistors Q1 and Q2 are perfectly matched, determine the value of V_{CE_Q} for both transistors respectively. [3]

Question 2

a. The midrange voltage gain of an amplifier is 250. The amplifier's input RC circuit model contributed a lower cutoff frequency of 500Hz and a 20dB/dec roll-off rate.

i. Determine the amplifier's voltage gain at 500Hz. [3]

ii. Determine the amplifier's voltage gain at 50Hz. [4]

iii. At what frequency will the amplifier exhibit unity gain? [4]

iv. How will you quantitatively modify the circuit if the lower cutoff frequency of the amplifier is to be reduced to 100Hz? [4]

b. Figure-Q2(b) shows a BJT based amplifier circuit. The transistor's $\beta = 100$ and $r_e = 16\Omega$.

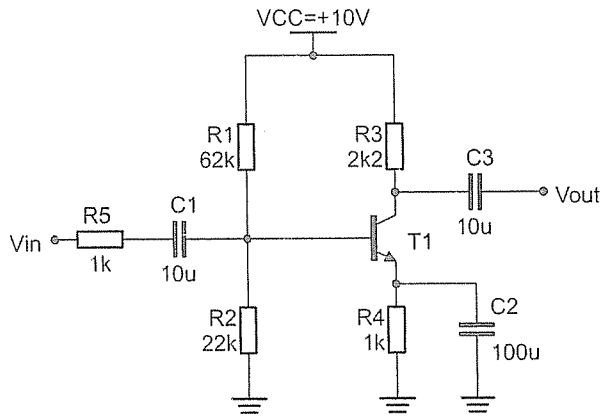

Figure-Q2(b)

i. Draw the AC equivalent model for the amplifier circuit in Figure-Q2(b), assuming only the bypass capacitor is acting alone. [4]

ii. Hence, determine the cutoff frequency contributed by the bypass capacitor. [6]

Question 3

a. i. Draw an op-amp based inverting amplifier circuit. [3]

ii. If the input resistance of the inverting amplifier circuit drawn in part 3(a)(i) is 27kΩ, while its feedback resistance is 470kΩ, what is the voltage gain of the amplifier? [3]

iii. What is the feedback factor of the inverting amplifier in part 3(a)(ii)? [3]

iv. If the connections of the input terminals of the op-amp in part 3(a)(ii) are swapped, what is the name of the circuit formed and quantitatively how will it affects the output waveform if a relatively large sinusoidal waveform is applied to the circuit. [6]

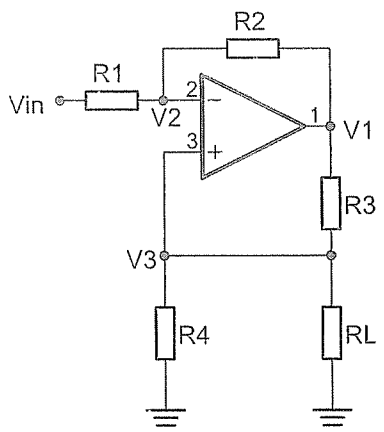

Figure-Q3(b)

b. i. Assume ideal op-amp operation, what is voltage relationship between V_2 and V_3 in Figure-Q3(b)? [1]

ii. Write the node equations for V_2 and V_3 respectively. [4]

iii. Hence show that the load current is directly proportional to the input voltage V_{in} and is independent of the load resistance R_L if $R_2R_4 = R_1R_3$. [5]

Question 4

a. The transfer function of an active filter is given as,

$$T(s)=\frac{100s^2}{s^2+141.421\pi s+10^4\pi^2}$$

i. What is the type of the filter? [2]

ii. Determine the cutoff frequency of the filter in Hz. [3]

iii. Determine the passband gain of the filter in dB unit. [3]

iv. What is the expected stopband roll-off rate of the filter? [2]

v. Determine the gain of the filter at 25Hz. [3]

vi. Does the filter exhibit any peaking in its frequency response? Why? [2]

b. Figure-Q4(b) shows an op-amp based active filter.

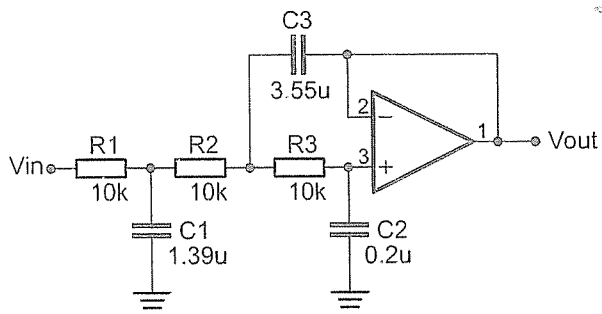

Figure-Q4(b)

i. What is the order of the filter? [2]

ii. Quantitatively show that the circuit in Figure-Q4(b) implements a low pass filter. [6]

iii. What is the passband gain of the filter? [2]

Question 5

a. The circuit in Figure-Q5(a) is intended to implement an oscillator circuit.

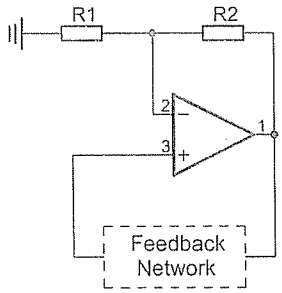

Figure-Q5(a)

i. Identify the circuit configuration formed by the op-amp, R_1 and R_2 in Figure-Q5(a). [2]

ii. Draw a circuit for the feedback network in Figure-Q5(a) to complete the oscillator circuit. [3]

iii. What is the phase-shift contributed by the feedback network drawn in part 5(a)(ii) if the oscillator circuit has sustain oscillation? [2]

iv. Explain the main problem in the given oscillator circuit. [3]

v. Suggest a solution to the problem explained in part 5(a)(iv). Support your solution with a clearly drawn schematic diagram. [5]

b. Figure-Q5(b) shows a first order active all pass filter.

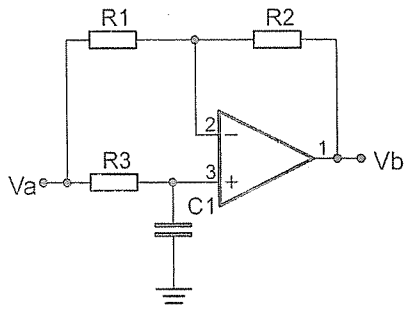

Figure-Q5(b)

i. Determine the phase shift expression of the circuit in Figure-Q5(b). [5]

ii. Explain how two of the circuit in Figure-Q5(b) can be utilized with an inverting amplifier to form a harmonic oscillator. Support your explanation with a clearly drawn schematic diagram. [5]

Question 6

a. Figure-Q6(a) shows a voltage regulator circuit using a 3-terminal IC voltage regulator.

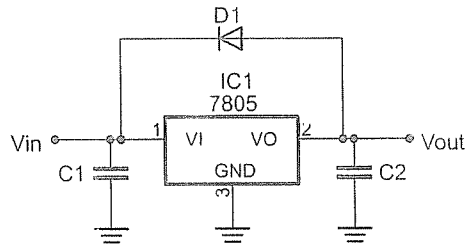

Figure-Q6(a)

i. State three advantages of the 3-terminal IC voltage regulator. [3]

ii. State the main disadvantage of the 3-terminal IC voltage regulator. [1]

iii. Explain the function of diode D_1. [3]

iv. If the IC voltage regulator has a line regulation given by 50mV/V, what does that mean? [3]

v. If the ground connection at pin-3 of IC1 is replaced by a 2V DC supply, what is the output voltage V_{out}? [3]

b. Figure-Q6(b) shows an application of a 3-terminal IC voltage regulator.

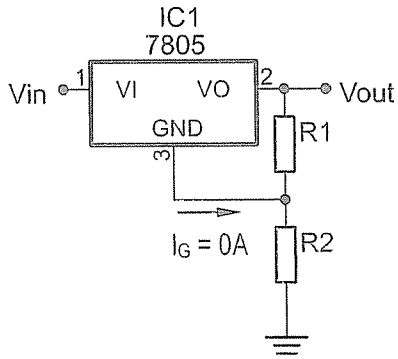

Figure-Q6(b)

i. If 0.8A is to be maintained flowing through resistor R_2 regardless of its non-zero and finite resistance, what should be the value of resistor R_1? [3]

ii. With the value of resistor R_1 obtained in part 6(b)(i), what is the current flowing through resistor R_2 if IC_1 is replaced with a 7808 regulator? [2]

c. Figure-Q6(c) shows a voltage regulator circuit.

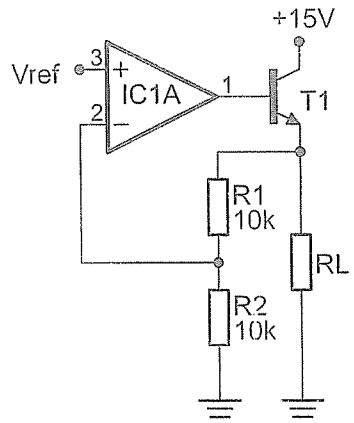

Figure-Q6(c)

i. If V_{ref} in Figure-Q6(c) is 5V, how much voltage drop across the load resistor R_L? [2]

ii. If resistor R_L in Figure-Q6(c) is 10kΩ while V_{ref} remains 5V, what is the approximated current drawn from the 15V source? State any assumption made. [3]

iii. How much current will be drawn from the 15V source if resistor R_2 is open-circuited while resistor R_L remains as 10kΩ and V_{ref} remains as 5V? [2]

– THE END –

EEE1103(F) / August-2012 / Chan Tse Wei / 080912