INTI
INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session : August 2012

Programme : DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING (DEEI)

Course : EEE1102 : ELECTRONIC DEVICES AND CIRCUIT THEORY I

Date of Examination : 11 December 2012

Time : 11a.m. – 1p.m. Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

Materials permitted :

Non Programmable Scientific Calculator

Materials provided :

Nil

Examiner(s) : Liong Han Wen

Moderator :

This paper consists of 7 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)

EEE 1102 : ELECTRONIC DEVICES AND CIRCUIT THEORY 1
FINAL EXAMINATION : AUGUST 2012 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in brackets at the right-hand margin.

Question 1

a. Find the average value of the full wave rectified voltage waveform as shown in Figure Q1(a). (5 marks)

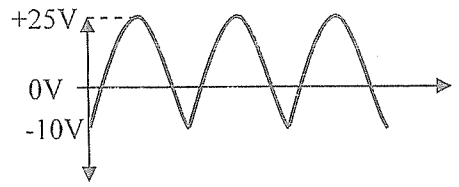


Figure Q1(a)

b. Explain what is intrinsic semiconductor. (2 marks)

c. Explain what is Peak Inverse Voltage (PIV) of a diode. (2 marks)

d. Determine the V_{OUT} for the circuit shown in Figure Q1(d). Assume all diodes are ideal. (4 marks)

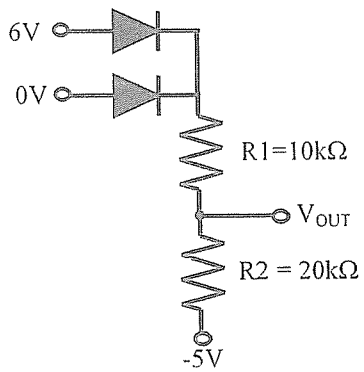


Figure Q1(d)

e. Sketch the block diagram for the internal function block of a of a basic DC voltage power supply with AC input voltage. Describe the function of each module. (12 marks)

Question 2

a. Sketch the output waveform(V_{OUT}) of the following rectifier circuits. The input waveform is shown in Figure Q2(a). Assume all the diodes in this part are ideal.

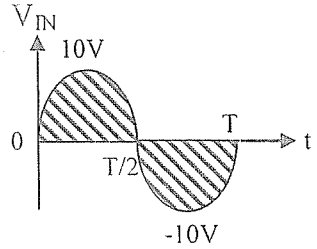
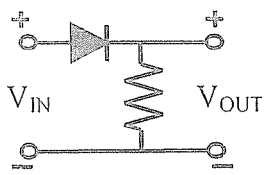
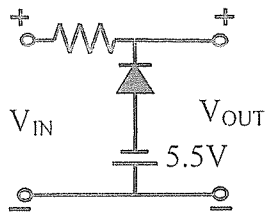


Figure Q2(a)

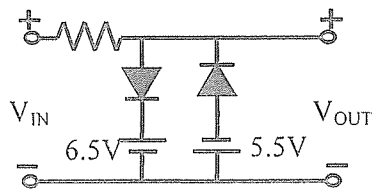
(i) (3 marks)



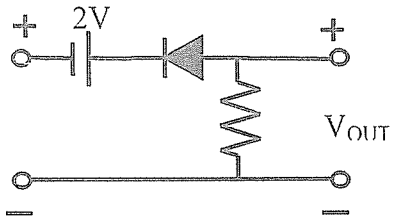
(ii) (5 marks)



(iii) (6 marks)



(iv) (5 marks)



b. For circuit shown in Figure Q2(b), to what value must R be adjusted in Figure below to make Iz = 50mA ? Assume Vz = 10V at 30mA and Zz = 40Ω. (6 marks)

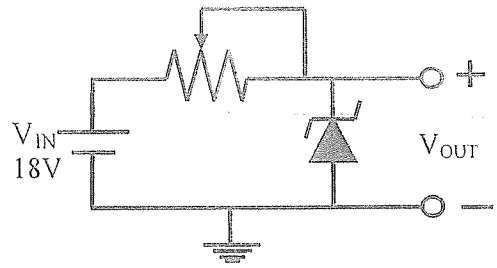


Figure Q2(b)

Question 3

a. Sketch a DC load line and AC load line for the circuit shown in Figure Q3(a) with a common graph. Assume β_{DC} and β_{ac} is equal to 100. (15 marks)

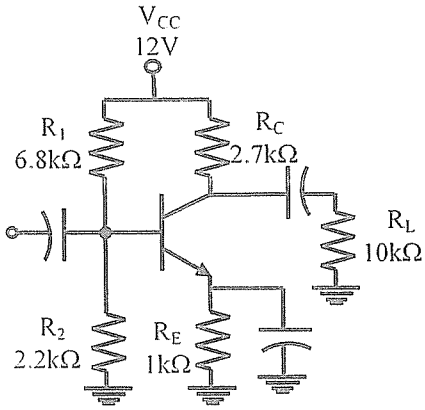


Figure Q3(a)

b. An npn transistor is to be operated at a collector current of 50mA. How high can V_{CE} be without exceeding a maximum power of 1.2W? (3 marks)

c. Determine the $I_{C(sat)}$ for the transistor in Figure Q3(c). What is the necessary value of I_B to produce saturation? What minimum value of V_{IN} is necessary for saturation? Assume $V_{CE(sat)} = 0V$. (7 marks)

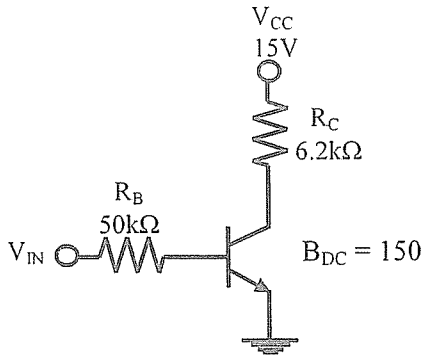


Figure Q3(c)

Question 4

a. The base bias circuit in Figure Q4(a) is subjected to a temperature variation from 0°C to 70°C. The β_{DC} decrease by 50 percent at 0°C and increase by 75 percent at 70°C from its nominal value of 110 at 25°C. What are the % of changes in I_C over the temperature change from 0°C to 70°C ? (7 marks)

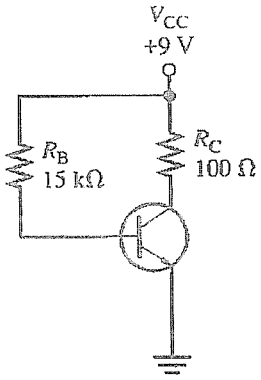


Figure Q4(a)

b. For the circuit shown in Figure Q4(b), find the value of R_B that will cause the transistor just in saturation. (9 marks)

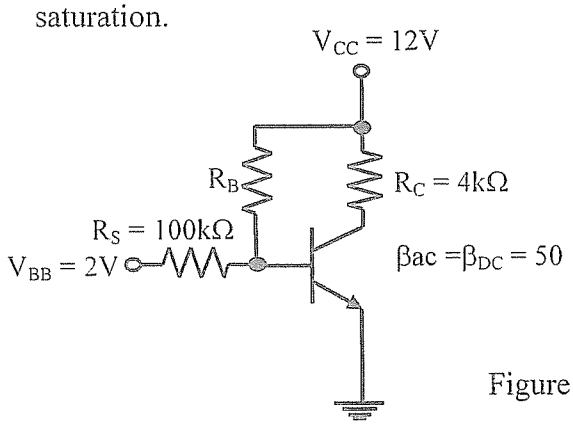


Figure Q4(b)

c. Determine the values of V_C and V_B for the network shown in Figure Q4(c). Assume β_{DC} =100. (9 marks)

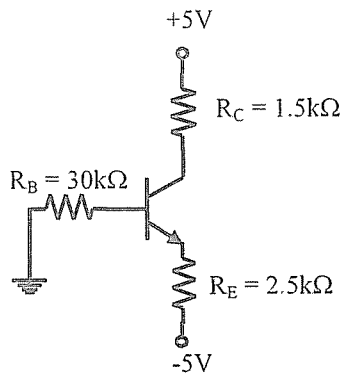
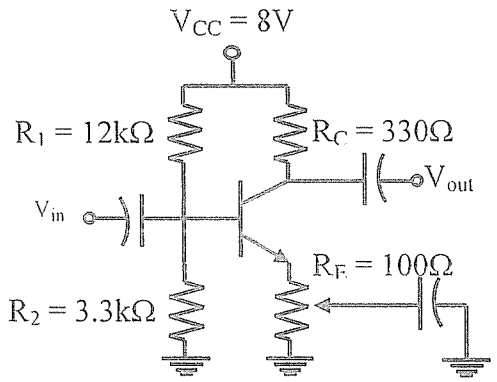


Figure Q4(c)

Question 5

a. The amplifier in Figure Q5 (a) has a variable gain control, using 100Ω potentiometer for R_E with wiper ac grounded. As the potentiometer is adjusted, more or less of R_E is bypassed to ground, thus varying the gain. The total R_E remains constant to dc, keeping the bias fixed. Determine the maximum and minimum gains for this unloaded amplifier. (14 marks)



$\beta_{DC} = 150$
$\beta_{ac} = 150$

Figure Q5(a)

b. For the transistor circuit shown in Figure Q5b, determine the DC value of :

i. I_E (4 marks)
ii. V_C (3 marks)
iii. V_{CE} (4 marks)

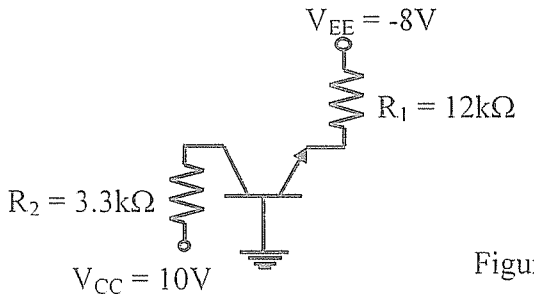


Figure Q5b

Question 6

a. Sketch the construction of Depletion MOSFET(both p and n channel). What is the difference in the operation of D-MOSFET and E-MOSFET? (6 marks)

b. Given a D-MOSFET with $I_{DSS} = 10mA$ and $V_{GS(off)} = -8V$.

(i) What type of the D-MOSFET is? Why? (2 marks)
(ii) Calculate I_D at $V_{GS} = -3V$ (2 marks)
(iii) Calculate I_D at $V_{GS} = +3V$ (2 marks)

c. What is the total output voltage of the unloaded amplifier shown in Figure Q6(c). Given I_D = 1.96mA. For this particular JFET, I_{DSS} is 12mA and $V_{GS(off)}$ is -3V. (8 marks)

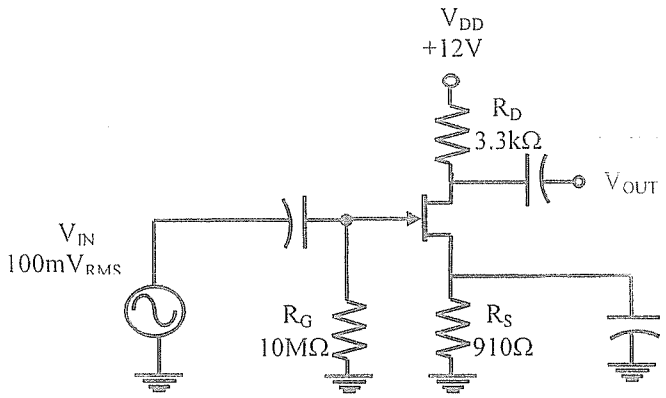


Figure Q6(c)

d. Find V_{GS} and V_{DS} for the E-MOSFET circuit in Figure Q6(d). Datasheet information is listed with the circuit. (5 marks)

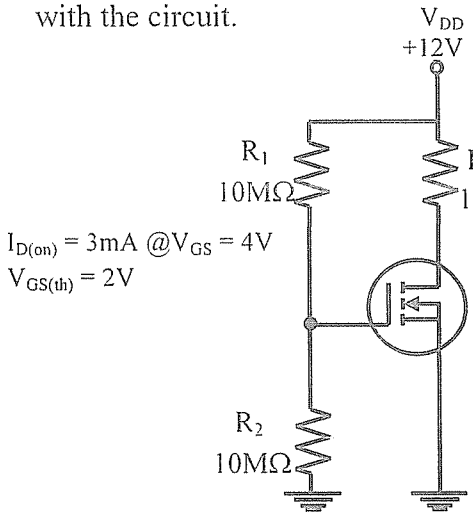


Figure Q6(d)

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