



**INTI**  
International College Penang  
LAUREATE INTERNATIONAL UNIVERSITIES\*

**FINAL**  
Examination Paper

(COVER PAGE)

Session : April 2017

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE 2101: Introduction To Digital Electronics

Date of Examination : 31 July 2017 (Monday)

Time : 11:00am – 1:00pm Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

**IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL**

Materials permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s) : Mr. Steven Khoo Boo Tap

Moderator : Mr. Kevin Tan Geok Su

*This paper consists of 10 printed pages, including the cover page.*

## INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)  
 EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS  
 FINAL EXAMINATION: APR2017 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

**Question 1**

A combinational logic circuit is required, which accepts BCD inputs 0000 to 1001 and displays the letter QRSTUVWXYZ, respectively, as shown below in Figure 1(a-1). The BCD inputs are labelled as  $P_1P_2P_3P_4$ ,  $P_1$  is the MSB and  $P_4$  is the LSB. Figure 1(a-2) shows a Common-Cathode 14 segment display. Assume all unused inputs as don't care.



Figure 1(a-1)

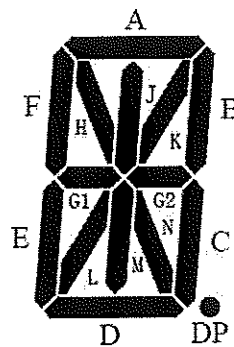


Figure 1(a-2)

- Develop the truth table for the inputs to segments A through N of the 14 segment. (7 marks)
- Determine the SOP form of the logic expression for segments A, F and K. (9 marks)
- Implement the logic expression of Segments A, F and K using only 2-input NOR gate with minimum 7402 ICs consideration. State the number of ICs used. Show all working clearly. (9 marks)

### Question 2

- (a) Design a synchronous 3-bit up/down Gray code counter using positive edge-triggered D flip-flop for MSB, JK flip-flop for next bit and RS flip-flop for LSB as shown in Figure 2(a). Assume  $D_A$  is the MSB input,  $J_B$  &  $K_B$  are the next flip-flop inputs and  $R_C$  &  $S_C$  are the LSB inputs. Input  $Z$  will be used as the up/down controller. The counter will count from  $000 \Rightarrow 001 \Rightarrow 011 \Rightarrow 010 \Rightarrow 110 \Rightarrow 111 \Rightarrow 101 \Rightarrow 100 \Rightarrow 000$  for counting up when input,  $Z = 0$  and  $000 \Rightarrow 100 \Rightarrow 101 \Rightarrow 111 \Rightarrow 110 \Rightarrow 010 \Rightarrow 011 \Rightarrow 001 \Rightarrow 000$  for counting down when input,  $Z = 1$ . Use  $Q_A Q_B Q_C$  outputs labelling for  $D_A$ ,  $J_B$  &  $K_B$  and  $R_C$  &  $S_C$  inputs. Provide proper labelling for the designed logic circuit. Show all workings clearly.
- Provide the excitation table used and the state diagram. (3 marks)
  - Provide the transition table/ next state table. (5 marks)
  - Simplify using Karnaugh map and Boolean algebra if necessary. (6 marks)
  - Draw the complete logic circuit diagram with proper label. (5 marks)

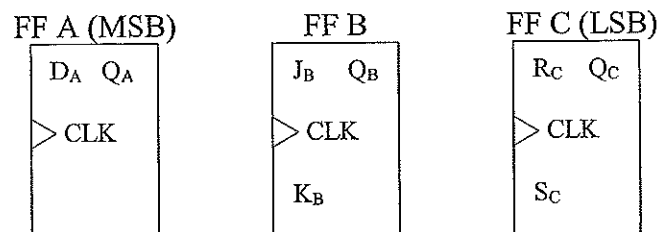


Figure 2(a)

- (b) A binary-weighted-input DAC is shown in Figure 2(b). If the LSB bit resistor has a value of  $240\text{k}\Omega$ , compute the values of the other input resistors. Also, calculate the  $V_{\text{out}}$  if the DAC has a binary input of 1011 with Logic 1 (HIGH) as  $+4.0\text{V}$  and Logic 0 (LOW) as  $0\text{V}$ . Assume that  $R_f$  equals to  $15\text{k}\Omega$ . What are the disadvantages of this method of DAC? (6 marks)

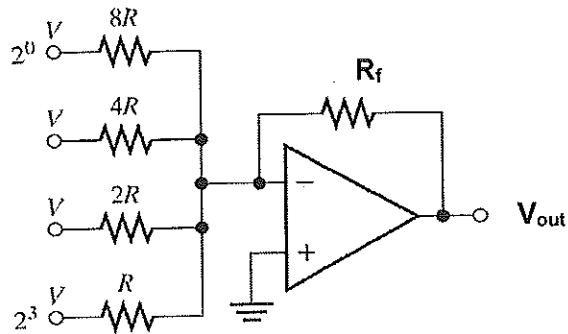


Figure 2(b)

**Question 3**

- (a) Table 3(a) and Table 3(b) show a portion of a dual positive edge-triggered JK flip-flops (DM7476) and a triple 3-input AND gate datasheet respectively. Figure 3(a) show the logic circuit diagram of an asynchronous counter which uses positive edge-triggered JK flip-flops with labelling of  $Q_A Q_B Q_C Q_D$  where  $Q_D$  is MSB and  $Q_A$  is LSB. Assume the environment is at  $T_A = 25^\circ\text{C}$  with  $V_{CC} = 5\text{V}$ .

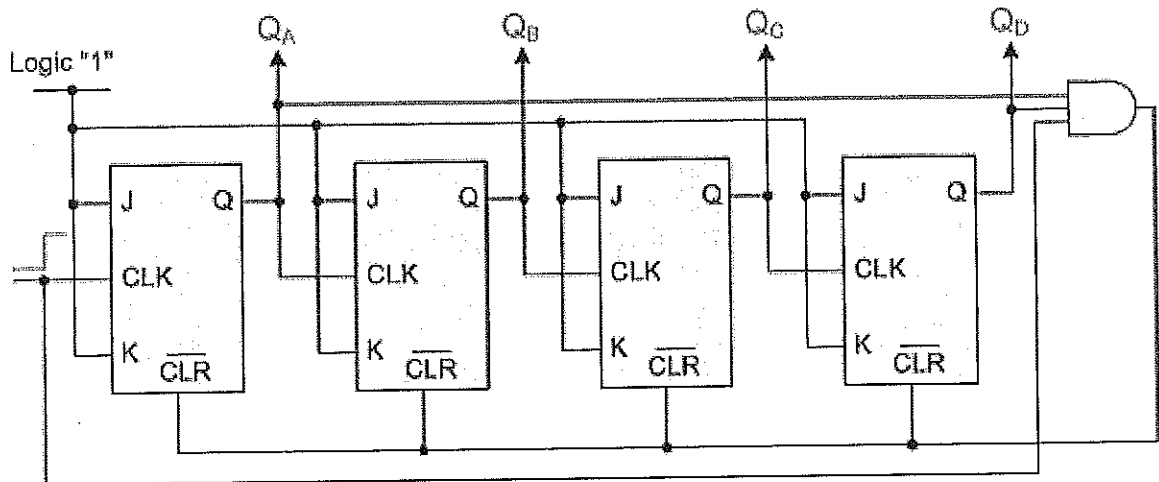


Figure 3(a)

Switching Characteristics					
at $V_{CC} = 5\text{V}$ and $T_A = 25^\circ\text{C}$					
Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega, C_L = 15\text{pF}$		Units
			Min	Max	
$f_{MAX}$	Maximum Clock Frequency		15		MHz
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Preset to $\bar{Q}$		40	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Preset to $Q$		25	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clear to $Q$		40	ns

$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\bar{Q}$		25	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\bar{Q}$		40	ns
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\bar{Q}$		25	ns

Table 3(a) JK flip-flop

Symbol	From (Input)	To (Output)	Test Conditions	Min	Typ	Max	Units
$t_{PLH}$	A, B or C	Y	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$		8	27	ns
$t_{PHL}$					10	19	ns

Table 3(b) AND gate

- (i) Determine the total propagation delay from the given datasheets in Table 3(a) and Table 3(b). (5 marks)
- (ii) Determine the maximum frequency at which the counter can be operated stably. (3 marks)
- (iii) Show the output timing diagram of Figure 3(a) and state the function of this counter. (5 marks)
- (b) Perform the following number system transformation. Show all workings clearly.
- (i)  $[102.5_{16} - 302.15_8]$  to BCD equivalent. (4 marks)
- (ii)  $[156.32_8 \times 12.5_8]$  to binary equivalent with 8 binary points accuracy. (4 marks)
- (iii)  $[163.0703125_{10} - 1001.001000001_2]$  to hexadecimal equivalent with 3 hexadecimal points accuracy. (4 marks)

**Question 4**

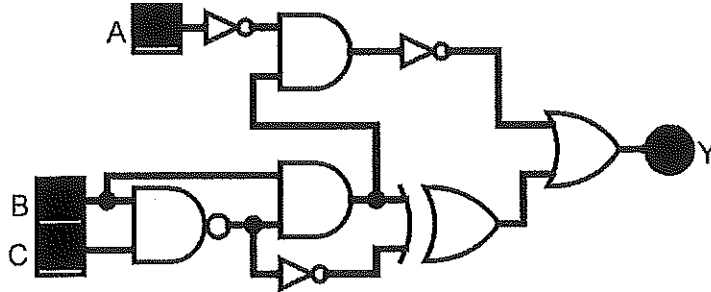
- (a) Using Boolean algebra only, simplify to the simplest logic gate(s):

(i)

$$Y = \overline{AC} \cdot \overline{ABC} \cdot \overline{B} + \overline{A} \cdot \overline{B} \cdot \overline{C}$$

(3 marks)

(ii)



(5 marks)

(b) Figure 4(b) below shows a 4-bit synchronous counter which is designed so that it performs a special counting sequence. Analyse its operation by determining its counting sequence. Assume that all flip-flops are initially in the 0 state (0000) for  $Q_3Q_2Q_1Q_0$ . Flip-flop FF3 is MSB and FF0 is LSB. Use  $J_3K_3$ ,  $J_2K_2$ ,  $J_1K_1$  and  $J_0K_0$  inputs labelling for  $Q_3$ ,  $Q_2$ ,  $Q_1$  and  $Q_0$  outputs. Show all workings clearly.

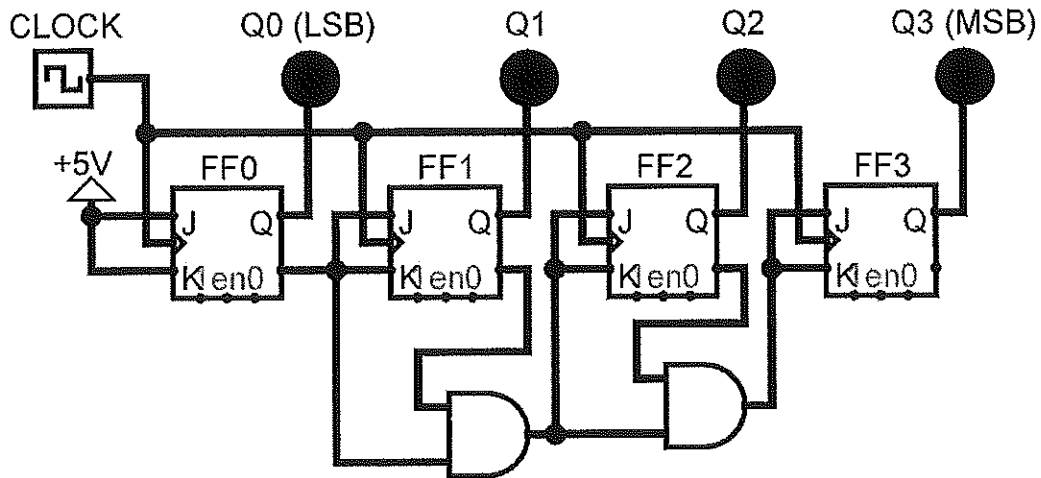


Figure 4(b)

- (i) Provide the Boolean expressions from the logic circuit. (4 marks)
- (ii) Provide all Karnaugh maps according to the expressions. (6 marks)
- (iii) Provide the transition table/ next state table with excitation table. (5 marks)
- (iv) Draw the state diagram and comment on the outcome of the states obtained. (2 marks)

**Question 5**

- (a) Use Karnaugh map or Boolean algebra to obtain the minimum SOP expression for the logic circuit.

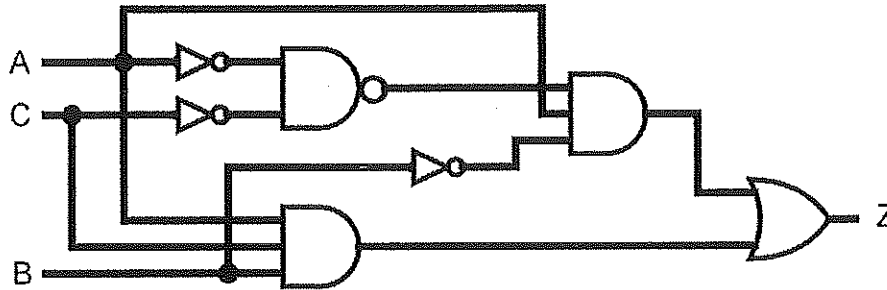


Figure 5(a)

(5 marks)

- (b) Figure 5(b) represents a multiplier circuit that takes 2-bit binary numbers  $X_1X_0$  and  $Y_1Y_0$  and produces an output binary number  $Z_3Z_2Z_1Z_0$ .

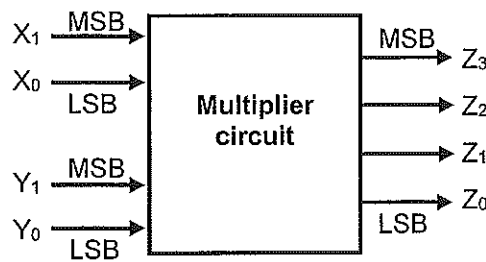


Figure 5(b)

Design the logic circuit for the Multiplier. Show all working clearly. Hint: The logic circuit will have four inputs and four outputs as shown in Table 5(b).

- (i) Complete the truth table below.

Input A		Input B		Output Z			
A <sub>1</sub>	A <sub>0</sub>	B <sub>1</sub>	B <sub>0</sub>	Z <sub>3</sub>	Z <sub>2</sub>	Z <sub>1</sub>	Z <sub>0</sub>
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Table 5(b)

(3 marks)

- (ii) Simplify the Boolean expression to the simplest form using Karnaugh map and/or Boolean algebra for output  $Z_3, Z_2, Z_1$  and  $Z_0$ . (8 marks)
- (iii) Implement the logic circuit of the simplest Boolean expression for  $Z_3, Z_2, Z_1$  and  $Z_0$  using only 2-input NAND gate IC (7400). State the number of IC(s) required for your design. (9 marks)

**Question 6**

- (a) Figure 6(a) has three inputs (A, B, C) and two outputs (Y, Z).  
 Table 6a(i) shows a portion of quadruple 2-input AND gates datasheet.  
 Table 6a(ii) shows a portion of quadruple 2-input OR gates datasheet.  
 Table 6a(iii) shows a portion of quadruple 2-input XOR gates datasheet.  
 Table 6a(iv) shows a portion of hex-tuple NOT gates datasheet.
  - (i) Using the datasheets given, determine the maximum propagation delay time. Show all working clearly. (6 marks)
  - (ii) What is maximum operating frequency that can be applied to this circuit without affecting the functionality of the circuit? State the function of this circuit. (4 marks)

Symbol	Parameter	Conditions	Min	Max	Units
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	$C_L = 15 \text{ pF}$ $R_L = 400\Omega$		27	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output			19	ns

Table 6a(i) AND gate

Symbol	Parameter	$R_L = 2 \text{ k}\Omega$				Units
		$C_L = 15 \text{ pF}$		$C_L = 50 \text{ pF}$		
		Min	Max	Min	Max	
$t_{PLH}$	Propagation Delay Time LOW-to-HIGH Level Output	3	11	4	15	ns
$t_{PHL}$	Propagation Delay Time HIGH-to-LOW Level Output	3	11	4	15	ns

Table 6a(ii) OR gate

Symbol	Parameter	Conditions	CL = 15 pF, RL = 400Ω		Units
			Min	Max	
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Other input LOW		23	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output			17	ns
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Other input HIGH		30	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output			22	ns

Table 6a(iii) XOR gate

Symbol	Parameter	R <sub>i</sub> = 2 kΩ				Units
		C <sub>i</sub> = 15 pF		C <sub>i</sub> = 50 pF		
		Min	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	3	10	4	15	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	3	10	4	15	ns

Table 6a(iv) NOT gate

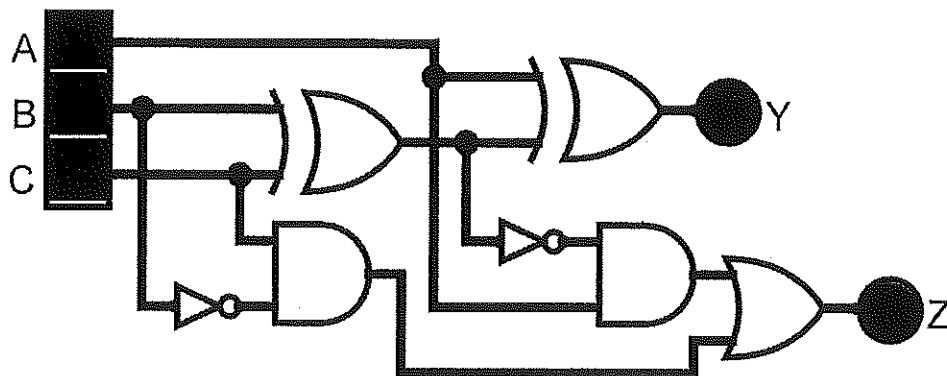


Figure 6(a)

- (b) A 14-bit DAC produces an output current in proportion to its digital input. For a digital input of 00000001010000, an output current of 75mA is produced.
- (i) What will the output current be if the digital input is 00100100011110? (3 marks)
  - (ii) What is the maximum output current produced by this DAC? (2 marks)
  - (iii) What should the digital input be if a 4.215A output current is required? (2 marks)

- (c) Table 6(c) shows the current ratings of TTL series logic gates. A 74F04 NOT gate output is driving 4 (FOUR) Standard TTL gate inputs, 7 (SEVEN) Advanced Low-Power Schottky TTL gate inputs, 3 (THREE) Advanced Schottky TTL gate inputs and 5 (FIVE) Low-Power Schottky TTL gate input as shown in Figure 6(c). Determine if there is a loading problem.

(8 marks)

TTL Series	Output Drive		Input Loading	
	$I_{OH}$	$I_{OL}$	$I_{IH}$	$I_{IL}$
74	400 $\mu$ A	16mA	40 $\mu$ A	1.6mA
74S	1.0mA	20mA	50 $\mu$ A	2.0mA
74LS	400 $\mu$ A	8mA	20 $\mu$ A	400 $\mu$ A
74AS	2.0mA	20mA	200 $\mu$ A	2.0mA
74ALS	400 $\mu$ A	8mA	20 $\mu$ A	100 $\mu$ A
74F	1.0mA	20mA	20 $\mu$ A	600 $\mu$ A

Table 6(c)

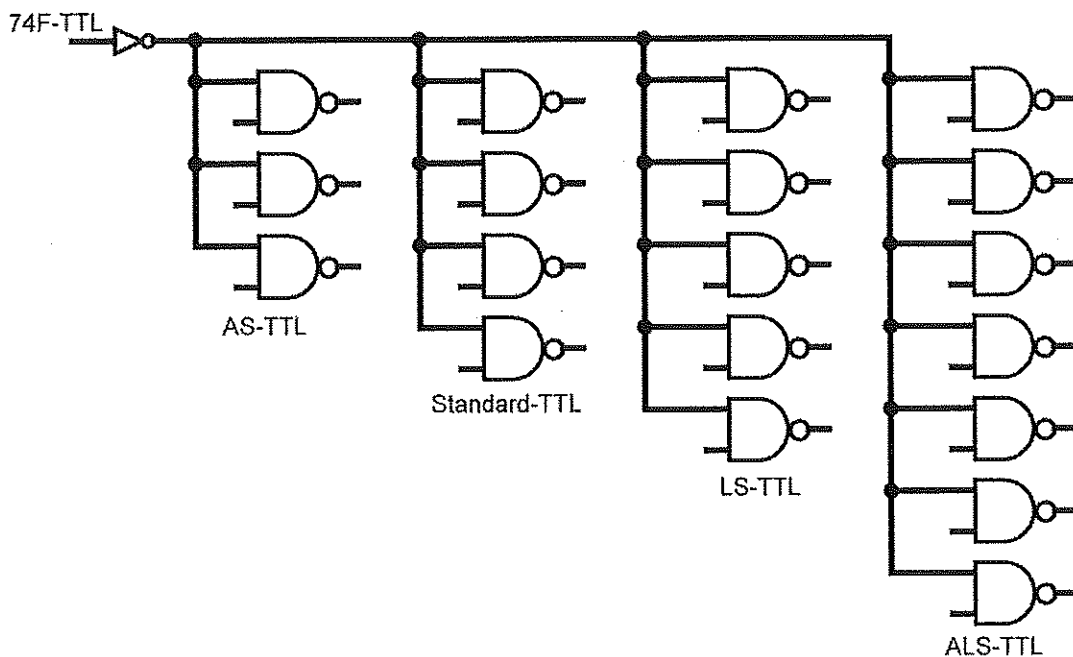


Figure 6(c)

– THE END –