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FINAL
Examination Paper

(COVER PAGE)

Session : **April 2017**

Programmes : Diploma in Electrical and Electronic Engineering (DEEI)

Course : **EEE1106: Analogue Electronics**

Date of Examination : 2 August 2017 (Wednesday)

Time : 11:00am – 1:00pm

Duration : 2 Hours Reading Time Nil

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL BY THE STUDENTS.

Materials Permitted : Scientific Calculator (Model fx570 Series)

Materials Provided : **WORKSHEET-Q6(a)**

Examiner(s) : **Chan Tse Wei**

Moderator : Dr. Khoo Bee Ee

This paper consists of 8 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
EEE1106: ANALOGUE ELECTRONICS
FINAL EXAMINATIONS: APRIL 2017 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks. The marks allocated to each sub-question are shown in square brackets at the right-hand margin. Present your answers neatly and clearly. The assessor reserves the rights to ignore your answers if they are ambiguous.

Question 1

a. i. "Common emitter amplifier and common source amplifier are classified as inverting amplifiers at mid-band frequency operation." Explain this statement. [3]

ii. If a common emitter amplifier has a voltage gain of 10 dB, determine its voltage gain in ratio of V_{out}/V_{in}. [3]

iii. An amplifier operating in single power supply mode must have its input and output coupled with capacitors. Explain the function of these coupling capacitor and state the drawback of having these capacitors in the amplifier circuit. [3]

iv. Explain the reasons for the voltage gain of an amplifier to reduce when it is operating in the high frequency spectrum. [3]

b. A bipolar junction transistor (BJT), when DC biased and operated with small input signals, can be modeled by a linear circuit shown in Figure-Q1(b)(i).

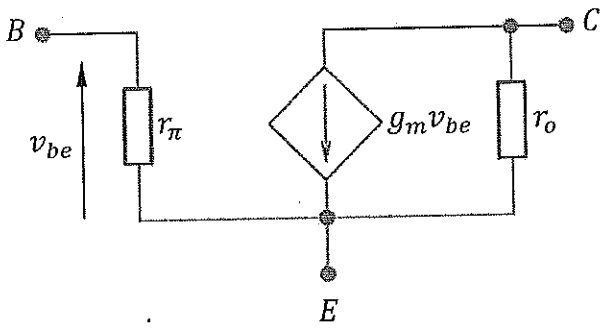

Figure-Q1(b)(i)

In the model (Figure-Q1(b)(i)),

r_π = input resistance between base and emitter = 2.5 $k\Omega$

g_m = short-circuit transconductance = 40 mS

r_o = output resistance = 100 $k\Omega$

The BJT is used in an amplifier circuit shown in Figure-Q1(b)(ii).

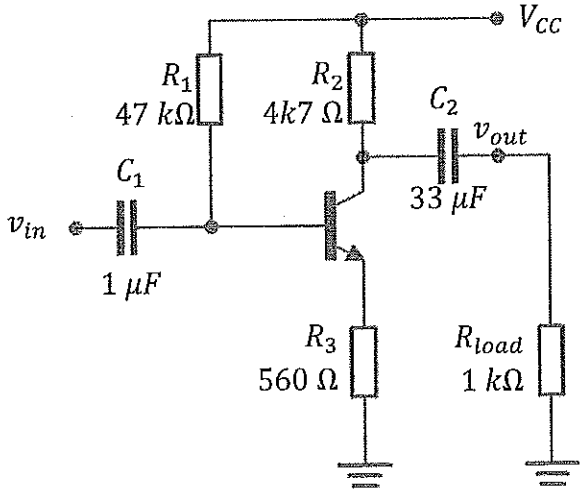

Figure-Q1(b)(ii)

i. Draw the a.c. equivalent circuit model for the amplifier circuit in Figure-Q1(b)(ii). [3]

ii. Calculate the maximum voltage gain of the amplifier. [10]

Question 2

a. i. Explain the importance of some power amplifiers to possess low output impedance characteristic. [3]

ii. Power amplifiers develop a.c. power of the order of a few watts, hence the transistors used in such amplifiers generate large amount of heat at their physical junctions. Explain the methods used to remove such heat build-up inside these devices. [3]

iii. A power amplifier delivers 10 W of a.c. power to a load by consuming 13 W of d.c. power from its voltage supplies. Calculate the power loss and power efficiency of the power amplifier. [3]

b. Figure-Q2(b) shows an a.c. load line of a class A power amplifier drawn on its power transistor output characteristic curves. Determine the maximum output power that can be delivered by the power amplifier. [4]

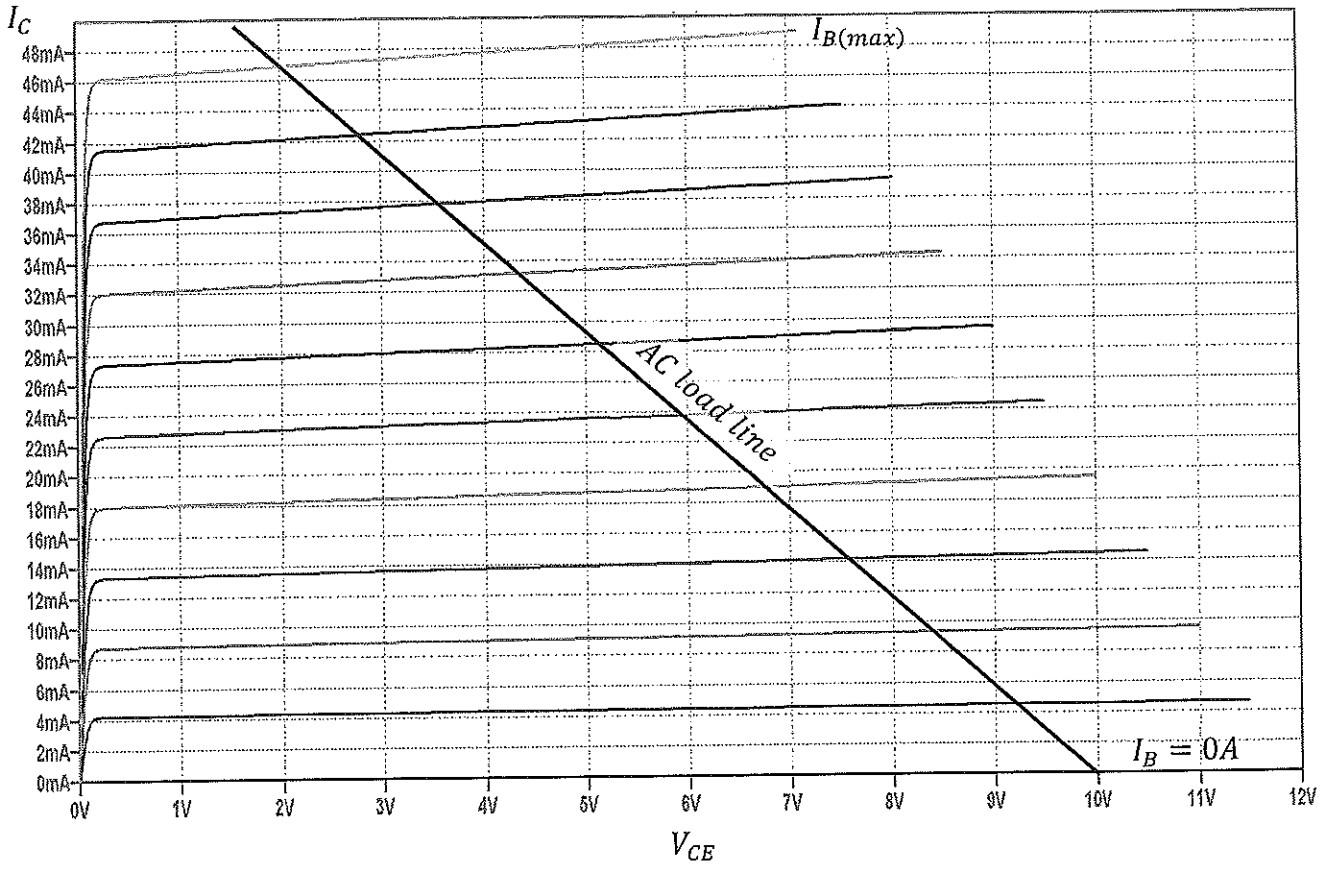

Figure-Q2(b)

c. Figure-Q2(c) shows a basic complementary pair push-pull class B power amplifier.
Under ideal transistor operations, its maximum input DC power is given by,

$$P_{DC} = \frac{2I_m}{\pi} V_{CC}$$

where I_m = peak current flowing through load resistor, R_L when v_{in} is a sinusoidal signal.
Whereas, the AC output power is given by,

$$P_{AC} = \frac{v_{out(rms)}^2}{R_L}$$

i. Show that the maximum ideal power efficiency of the power amplifier is 78.5%. [4]

ii. Show that the maximum ideal transistor power dissipation occurs when,

$$v_{out(max)} = \frac{2}{\pi} V_{CC}$$ [4]

iii. Show that the maximum ideal power efficiency of the power amplifier during maximum transistor power dissipation is 50%. [4]

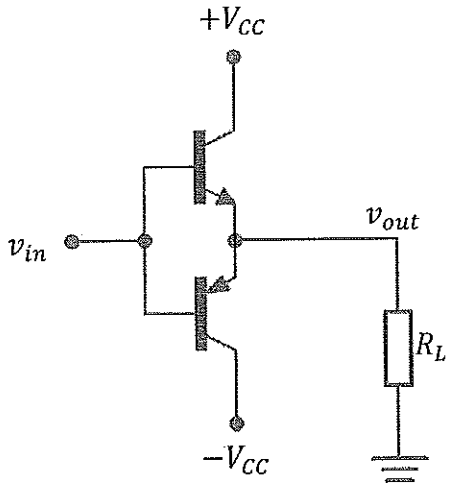

Figure-Q2(c)

Question 3

a. i. If an op-amp circuit needs to be operated in single supply mode, explain one relevant selection criteria for the op-amp in such an application. [3]

ii. Explain the need of negative feedback in most of the op-amp circuits. [3]

iii. Explain the meaning of op-amp output saturation. [3]

b. Design an inverting amplifier using a single op-amp that comply to the following specifications:

- Voltage gain = 35.563 dB
- Input resistance = 2 $k\Omega$

[6]

c. Design an op-amp based amplifier circuit that allows gain adjustment from -4 to $+4$ using a potentiometer. Quantitatively justify your design. [10]

Question 4

a. The transfer function of an active filter is given by,

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{15s}{s^2 + 3s + 700}$$

i. State the type of the given filter. [2]

ii. Calculate the maximum gain of the filter. [3]

iii. Calculate the Q-factor of the filter. [3]

iv. Calculate the frequency value (in Hz) that receives the highest amplification. [3]

v. Suggest an op-amp circuit, when cascaded with this active filter, will form a second order high pass filter. Quantitatively justify your suggestion. [4]

b. Figure-Q4(b) shows an active filter circuit implemented using equal value resistors and capacitors respectively.

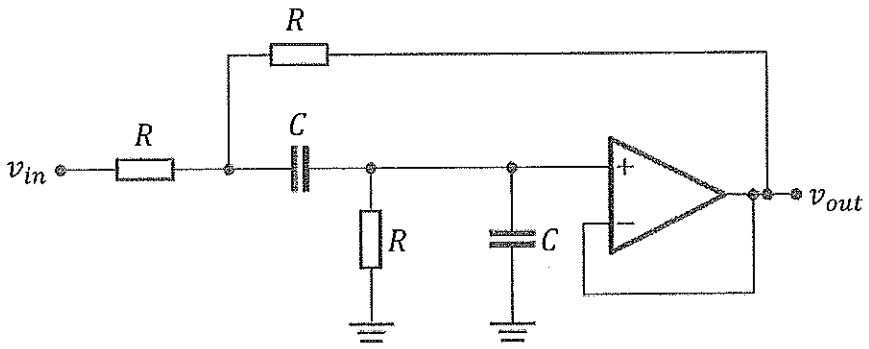

Figure-Q4(b)

Quantitatively show that the active filter has $Q = 0.354$ and its maximum output voltage is $0.25v_{in}$. [10]

Question 5

a. Figure-Q5(a) shows a block diagram of a circuit with positive feedback.

i. Derive the transfer function of the circuit, v_{out}/v_{in} in terms of A and β. [3]

ii. From the transfer function obtained in part (a)(i), determine the condition where the circuit generates an oscillating signal without the presence of any input voltage. [3]

iii. From the condition obtained in part (a)(ii), calculate the transfer function of A if $\beta = 0.4\angle 30°$. [3]

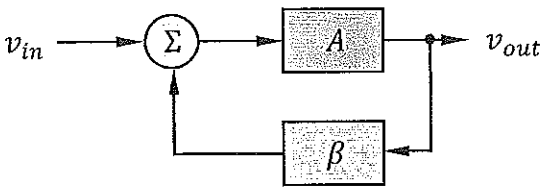

Figure-Q5(a)

b. Figure-Q5(b) shows a relaxation oscillator circuit.

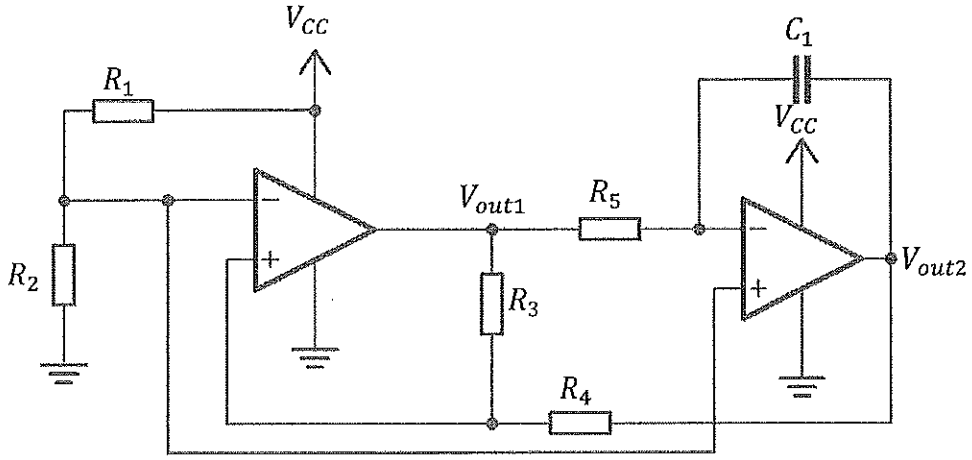

Figure-Q5(b)

i. Explain the meaning of relaxation oscillator circuit. [2]

ii. State the type of output signals generated at nodes V_{out1} and V_{out2}. [4]

iii. Explain the function of resistors R_1 and R_2 in the circuit. [3]

iv. Explain the effect of the value of capacitor C_1 on the oscillation frequency of V_{out1} and V_{out2}. [3]

v. If the oscillator circuit is designed with the following set up and the op-amps are assumed ideal, determine the peak-to-peak voltage of V_{out2}.

- $V_{CC} = 5\ V$
- $R_1 = R_2$
- $R_3 = 100\ k\Omega$
- $R_4 = 47\ k\Omega$

[4]

Question 6

a. Figure-Q6(a) shows an inverting amplifier circuit. Worksheet-Q6(a) shows the timing diagram of $v_{in}(t)$. Complete Worksheet-Q6(a) by drawing the waveforms of $v_{out}(t)$ and $v_x(t)$. Assume ideal op-amp operation. Justify your answers. [15]

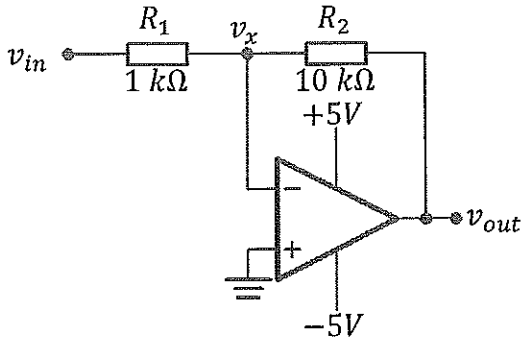

Figure-Q6(a)

b. Figure-Q6(b) shows an op-amp circuit that regulate the voltage across a load resistor.

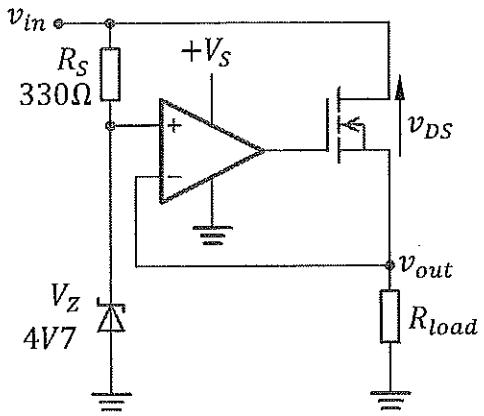

Figure-Q6(b)

i. State the voltage across R_{load}. [2]

ii. State the function of the n-channel MOSFET in the circuit. [3]

iii. State the minimum value of v_{in} to sustain voltage regulation if the zener diode has a nominal current of 2 mA. [3]

iv. If $v_{in} = 10.5\ V$, calculate the voltage across the n-channel MOSFET, v_{DS}. [2]

~ The End ~