



FINAL
Examination Paper

(COVER PAGE)

Session : April 2017

Programme : Diploma in Electrical and Electronic Engineering (DEEI)

Course : EEE 1105: Circuit Theory & Electronic Devices

Date of Examination : 3 August 2017 (Thursday)

Time : 11:00am – 1:00pm Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of SIX (6) questions. Answer any FOUR (4) questions in the answer booklet provided. All questions carry equal marks.

IMPORTANT NOTE : THIS PAPER SHOULD NOT BE TAKEN OUT OF THE EXAMINATION HALL

Materials permitted : Non-Programmable Scientific Calculator

Materials provided : Nil

Examiner(s) : Mr. Steven Khoo Boo Tap

Moderator : Mr. Kevin Tan Geok Su

This paper consists of 10 printed pages, including the cover page.

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DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEEI)
 EEE1105: CIRCUIT THEORY & ELECTRONIC DEVICES
 FINAL EXAMINATION: APR2017 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

- (a) Find the current passing through $15\ \Omega$ resistor using Nodal analysis and Thévenin's theorem for the circuit shown in Figure 1(a). (15 marks)

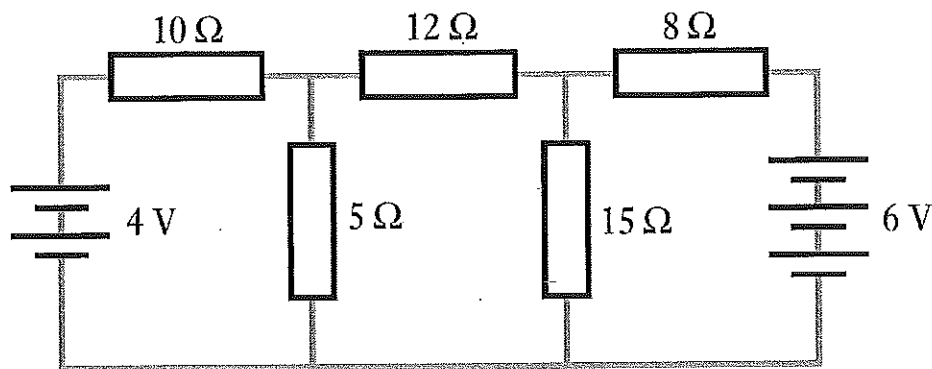


Figure 1(a)

- (b) Calculate the resistance and the inductance or capacitance in series for each of the following impedances:

Assume that the frequency is 50 Hz.

- (i) $10 + j15\ \Omega$. (2 marks)
- (ii) $-j80\ \Omega$. (2 marks)
- (iii) $50\angle 30^\circ\ \Omega$. (3 marks)
- (iv) $120\angle -60^\circ\ \Omega$. (3 marks)

Question 2

(a) A circuit as shown in Figure 2(a) having a resistance of $12\ \Omega$, an inductance of $0.15\ \text{H}$ and a capacitance of $100\ \mu\text{F}$ in series, is connected across a $100\ \text{V}$, $50\ \text{Hz}$ supply. Calculate:

- (i) the impedance; (4 marks)
- (ii) the current; (2 marks)
- (iii) the voltages across R , L and C ; (6 marks)
- (iv) the phase difference between the current and the supply voltage. (3 marks)

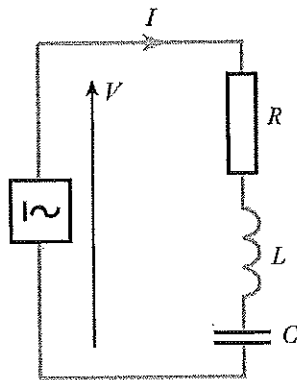


Figure 2(a)

(b) A network is arranged as in Figure 2(b). Calculate the equivalent resistance between node A and B.

(10 marks)

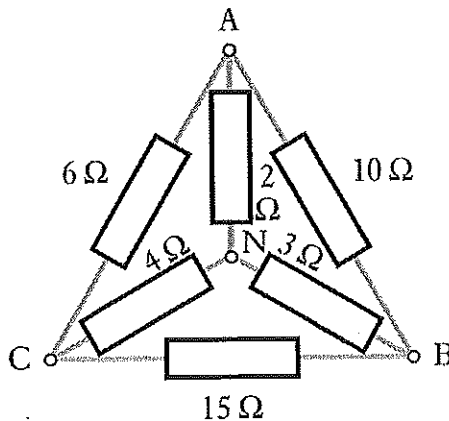
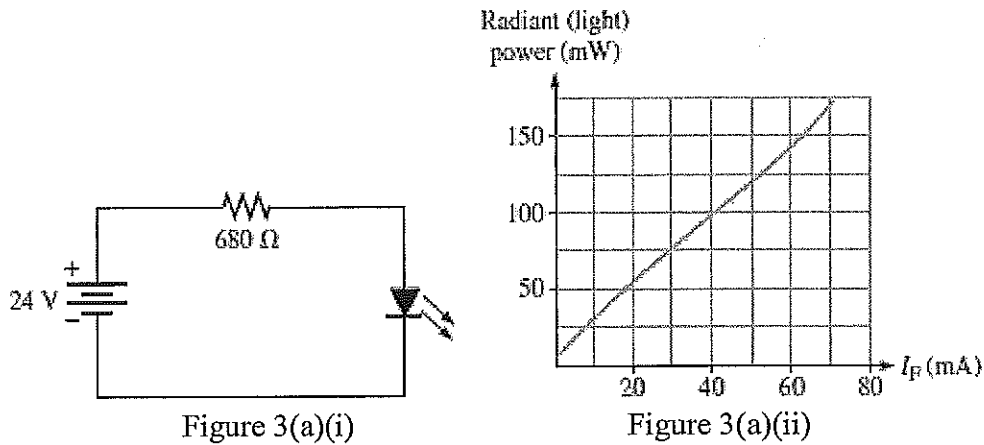


Figure 2(b)

Question 3

- (a) The LED in Figure 3(a)(i) has a light-producing characteristic of Radiant power versus forward current, I_F as shown in Figure 3(a)(ii). Assuming the forward voltage drop of the LED is 1.2 V, determine the amount of radiant (light) power produced in mW. (5 marks)



- (b) For the Zener diode network of Figure 3(b), determine V_L , V_R , I_Z and P_Z . What happens when the load resistance, R_L changed with 3 kΩ? (10 marks)

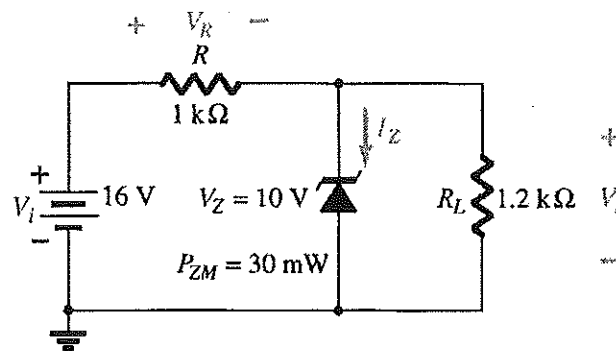


Figure 3(b)

- (c) Referring to Figure 3(c), determine:
- (i) the voltages at references V_{01} and V_{02} . (4 marks)
 - (ii) the current through LED and the power delivered by the supply. (3 marks)
 - (iii) the power absorbed by the LED compare to that 6 V Zener diode. (3 marks)

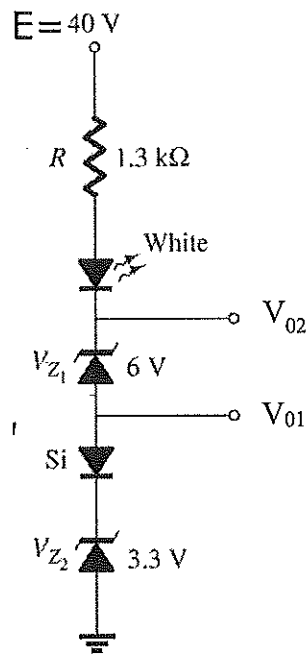


Figure 3(c)

Question 4

- (a) Briefly describe the three regions of BJT operation and the corresponding application. (3 marks)
- (b) For the circuit shown in Figure 4(b), find I_C and V_{CE} . Next, sketch the load line with proper labeling. (8 marks)

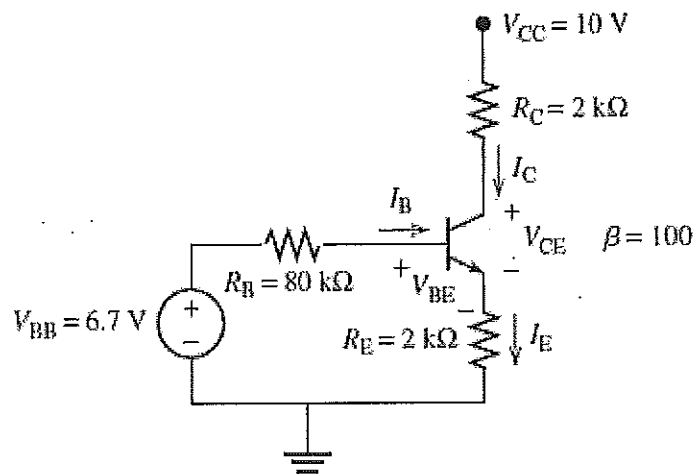


Figure 4(b)

- (c) Given the transistor inverter of Figure 4(c) to operate with a saturation current of 8 mA using a transistor with a $\beta = 100$. Use a level of I_B equal to 120% of I_{Bmax} calculate the value of R_C and R_B .

(5 marks)

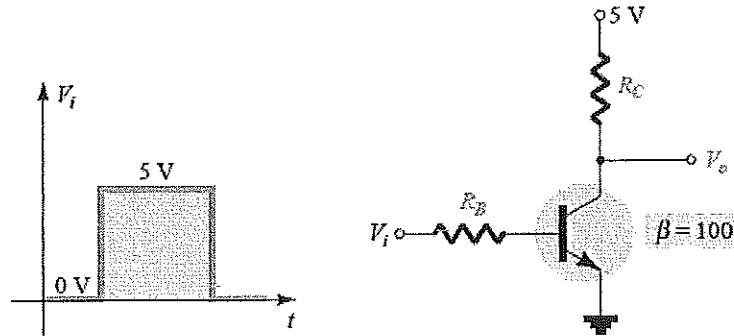


Figure 4(c)

- (d) Determine how much the Q-point (I_E , V_{CE}) for the circuit in Figure 4(d). Assume $V_{BE} = 0.7$ V and $\beta = 100$. Given $V_{CC} = 12$ V, $R_1 = 30$ k Ω , $R_2 = 10$ k Ω , $R_C = 1$ k Ω and $R_E = 0.5$ k Ω .

(9 marks)

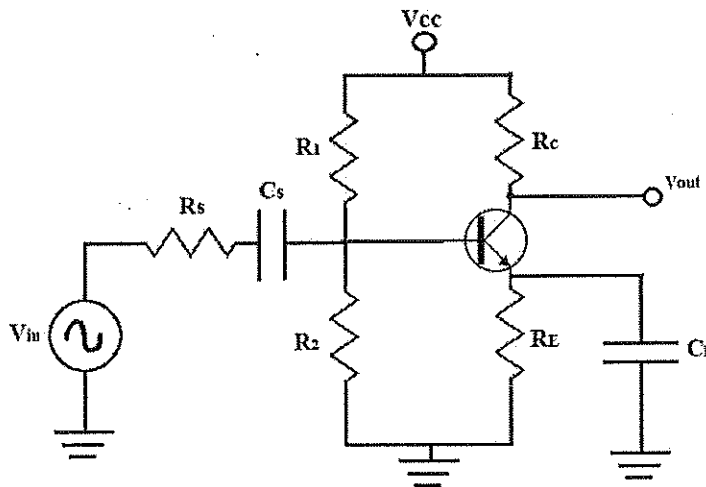


Figure 4(d)

Question 5

- (a) Three branches, possessing a resistance of 50Ω , an inductance of 0.15H and a capacitance of $100 \mu\text{F}$ respectively, are connected in parallel across a 100 V , 50 Hz supply. Calculate:
- The current in each branch. (3 marks)
 - The supply current. (2 marks)
 - The phase angle between the supply current and the supply voltage. (3 marks)

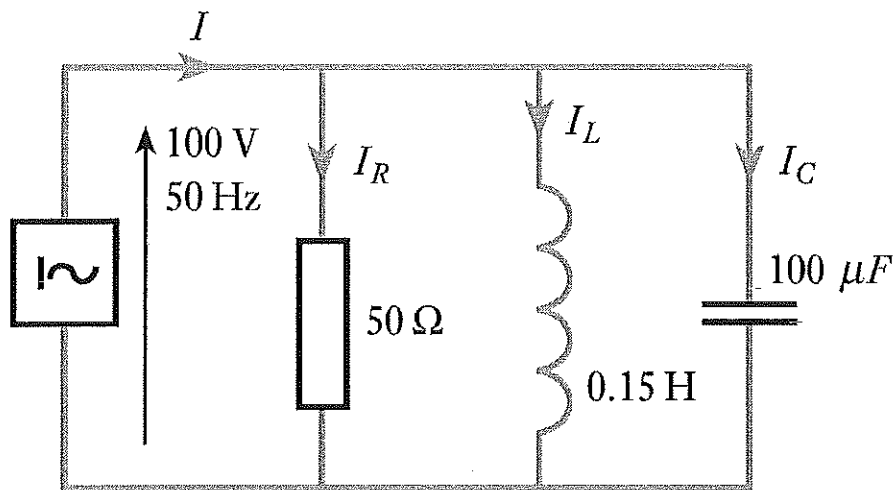


Figure 5(a)

- (b) The following graph in Figure 5(b) were obtained during an experiment on an N-channel FET. A FET operates with a drain current of 50 mA and a gate-source bias of -2 V . The forward transfer conductance, $g_{fs} = 0.025 \text{ S}$. Determine the change in drain current if the bias voltage increases to -2.5 V . (5 marks)

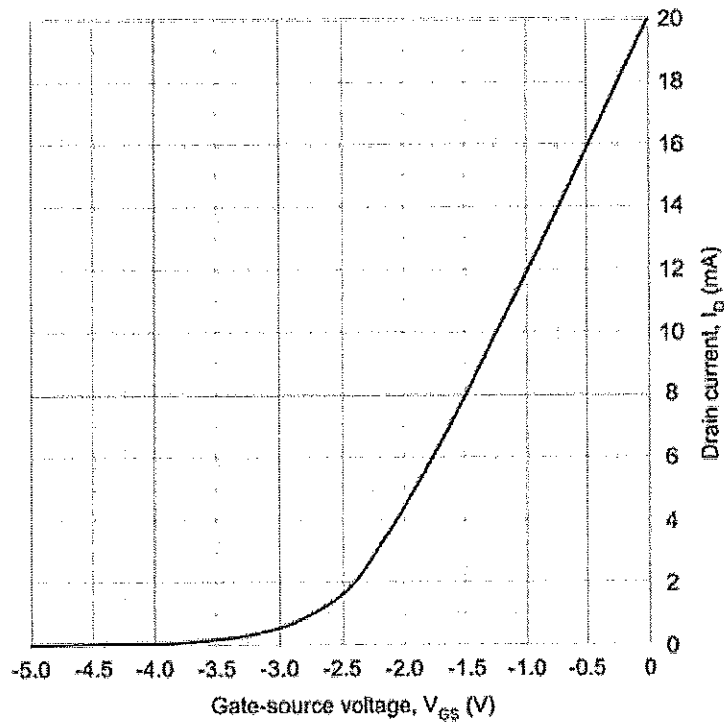


Figure 5(b)

(c) For the JFET biasing network in Figure 5(c), determine:

(i) The I_{DQ} and V_{GSQ} .

(8 marks)

(ii) The V_{DS} and V_{DG} .

(4 marks)

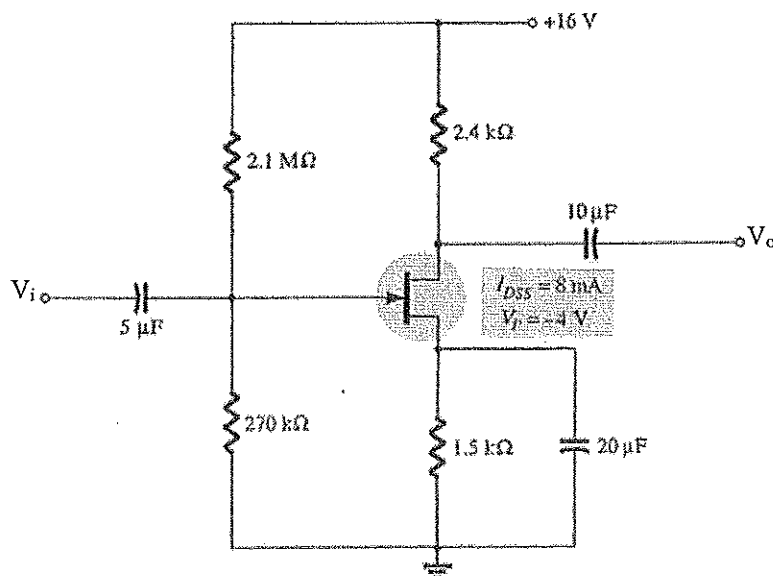


Figure 5(c)

Question 6

- (a) Calculate the voltage drops across all components in the circuit in Figure 6(a), expressing them in complex (polar) form with magnitudes and phase angles each. (6 marks)

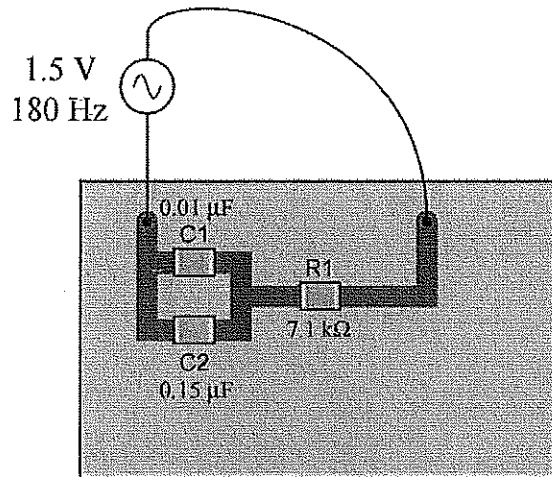


Figure 6(a)

- (b) Determine the total current and all component currents in the circuit in Figure 6(b). Also, calculate the phase angle (θ) between voltage and current in this circuit.

Given:

$L_1 = 1.2 \text{ H}$, $L_2 = 650 \text{ mH}$, $R_1 = 33 \text{ k}\Omega$, $R_2 = 27 \text{ k}\Omega$, $V_{\text{supply}} = 19.7 \text{ V}_{\text{RMS}}$, Frequency supply = 4.5 kHz .

(6 marks)

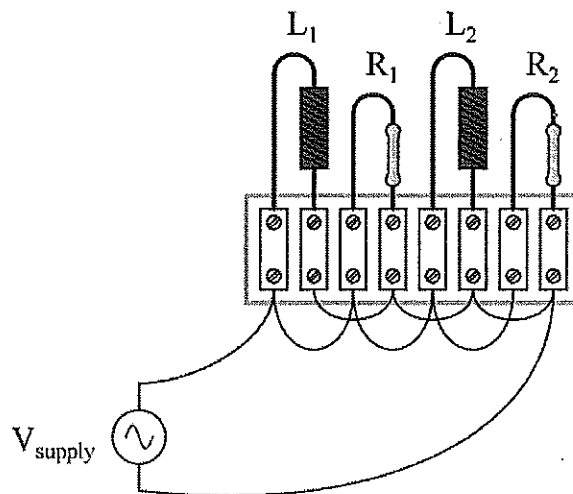


Figure 6(b)

- (c) Calculate the current in the $5\ \Omega$ resistor in the network shown in Figure 6(c) using Norton's theorem.

(6 marks)

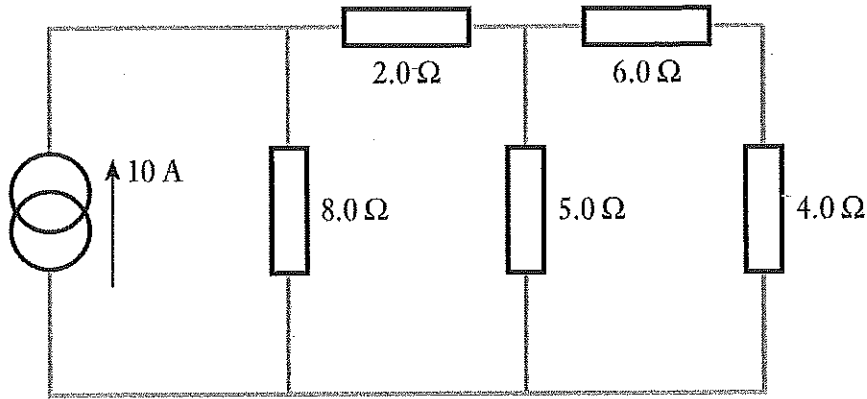


Figure 6(c)

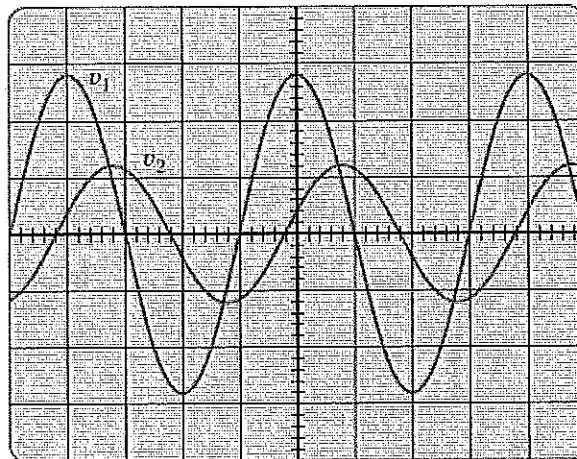
- (d) For the waveforms shown by the oscilloscope in Figure 6(d),

- (i) determine the phase relationship between the waveforms, and indicate which one leads or lags.

(4 marks)

- (ii) determine the rms value and frequency of each waveform.

(3 marks)



Vertical sensitivity = $0.5\ \text{V/div}$.
Horizontal sensitivity = $0.2\ \text{ms/div}$.

Figure 6(d)

– THE END –