INTI
INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session	:	APR 2014
Programme	:	DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING
Course	:	**EEE 2105: INTRODUCTION TO MICROPROCESSOR**
Date of Examination	:	25 JULY 2014
Time	:	5.00pm – 7.00pm Reading Time : Nil
Duration	:	2 Hours
Special Instructions	:	

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove the question papers from the examination venue.

Students are also not allowed to write anything on the Appendix handout given.

Materials permitted :

Non-Programmable Scientific Calculator

Materials provided :

Appendix A (8086 Instruction Set Summary), Appendix B (ASCII Table),
Appendix C (8255 PPI), Appendix D (8253/8254 PIT), Appendix E (8259 PIC)

Examiner(s)	:	**Steven Khoo**
Moderator	:	**Dr. Mandeep Singh**

This paper consists of 12 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

EEE2105: INTRODUCTION TO MICROPROCESSORS
FINAL EXAMINATION: APR2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

(a) Given the registers and the memory locations contents of 8086 as follows: (All values are in Hexadecimal).

Registers					
AX	1234H	CS	3010H	DI	0555H
BX	0404H	DS	5F41H	SI	5060H
CX	5678H	SS	5F81H	BP	6070H
DX	789AH	ES	7040H	IP	7100H

Memory															
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
5F800H	11	22	33	44	55	66	77	88	99	00	A1	B1	C1	D1	E1	F1
5F810H	02	04	45	78	90	11	22	33	44	55	66	77	88	99	00	12
5F820H	34	56	78	90	12	34	56	78	90	12	34	56	78	90	11	22
5F830H	33	44	55	66	77	88	99	00	10	A0	12	34	56	78	9A	BC
5F840H	DE	F0	00	11	00	11	10	21	99	B8	77	33	58	45	33	22
5F850H	25	31	19	00	01	22	20	31	89	C8	66	22	CC	54	44	06
5F860H	DC	F0	20	18	02	33	30	41	79	D8	55	11	BB	67	55	20
5F870H	FE	F1	10	12	03	44	40	51	69	E8	44	AA	55	76	66	21
5F880H	00	FF	00	FF	00	FF	00	60	5F	FF	14	00	FF	F1	80	09

Perform the following operations. Indicate the result in the register and the content where it is stored. The operations are independent of each other. Show all workings of before and after with appropriate diagram illustration.

(i) SUB [0416H – 32], DX

(3 marks)

(ii) OR [BP] + 23 + 23H – 60213o, BH

(3 marks)

(iii) ADD [DI] + 101b + 101o – 101 – 101H, AX

(3 marks)

(iv) AND [SI + BP + 0EB0H – BFADH + 10010000b], CX

(3 marks)

(v) XOR [BX], BX

(3 marks)

(b) Figure 1(b-1) shows a TM497BBK32 Dynamic RAM Module pin configuration.
Figure 1(b-2) shows a TM124GU8A Dynamic RAM Module pin configuration.

Determine the following:

(i) total memory capacity from RAMs in Kbits,

(4 marks)

(ii) individual memory organization,

(2 marks)

(iii) number of address pins and number of data pins of each RAM Module.

(4 marks)

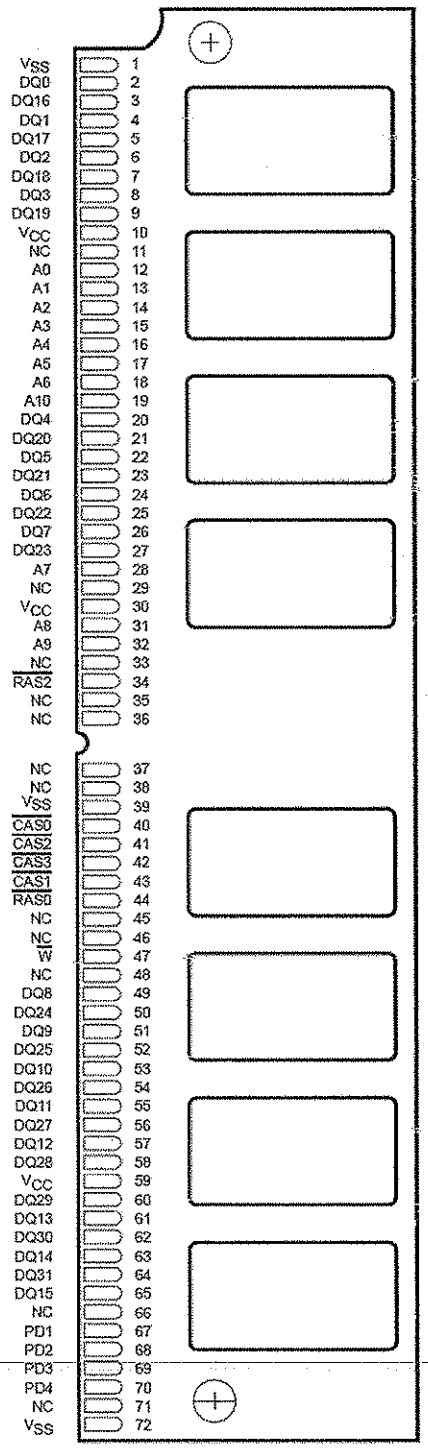

Figure 1(b-1) Pin configuration

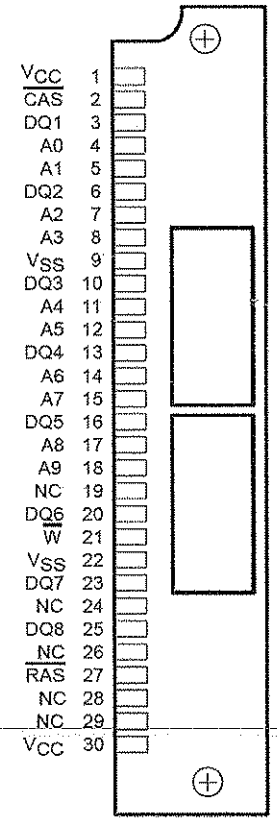

Figure 1(b-2) Pin configuration

Question 2

Study and analyze the 8086 Assembly Language Codes below and answer the following questions.

Line 1	TITLE SAMPLE PROGRAM
Line 2	.MODEL SMALL
Line 3	.STACK 64
Line 4	.CODE
Line 5	.DATA
Line 6	MYCODE PROC
Line 7	MOV AX, 04
Line 8	MOV BX, 0212
Line 9	CMP AX, BX
Line 10	JG action1
Line 11	JLE action2
Line 12	action1:
Line 13	ADD AL, 30
Line 14	JMP exit
Line 15	action2:
Line 16	ADD BL, 20
Line 17	JMP exitt
Line 18	exit:
Line 19	MOV AH, 4CL
Line 20	INT 21H
Line 21	MYCODE ENDP
Line 22	END MYCODE

Table 2 Coding

(a) Identify THREE (3) errors in the above instructions. Briefly explain why it is incorrect and write the correct codes according to the Assembly Language.

(9 marks)

(b) What is the meaning of the instruction at Line 10 and 11? Can these instructions be reduced?

(6 marks)

(c) What is the meaning of the combined instructions at lines 18, 19 and 20?

(6 marks)

(d) Based on the assumption that all lines of codes are corrected, what is the final outcome of the above program?

(4 marks)

Question 3

(a) Define the following function and how the function differs from their functionality.

(i) MUL & IMUL

(2 marks)

(ii) XOR & OR

(2 marks)

(b) (i) What is the 2's complement number of -3.625_{10} in signed numbering system?

(2 marks)

(ii) Determine the result of $2.25_{10} + (-4.75_{10})$ using 2's complement method.

(4 marks)

(iii) Prove that the final result is equal to -2.5_{10} in binary equivalents. Show all calculations working clearly.

(2 marks)

(c) The 8255 PPI is configured as shown in Figure 3(c).

(i) Find the port addresses and control register in Figure 3(c). Thus, program the PPI to set PC5 to high. Also include comments for any instruction used.

(5 marks)

(ii) Write a program to count the number of 1s from the data received at port A continuously via 8255 PPI. If the data is a positive number, send 44H to port B but if the data is a negative number, send 88H to port C. Also, include comments for any instruction used.

Examples of incoming data and the respective action:

- 25_H (Positive Signed Number) ⇨ send 44_H out to port B
- ED_H (Negative Signed Number) ⇨ send 88_H out to port C
- 00H (Positive Signed Number) ⇨ send 44_H out to port B
- 90_H (Negative Signed Number) ⇨ send 88_H out to port C

(8 marks)

[Refer to Appendix C for 8255 PPI Control Word]

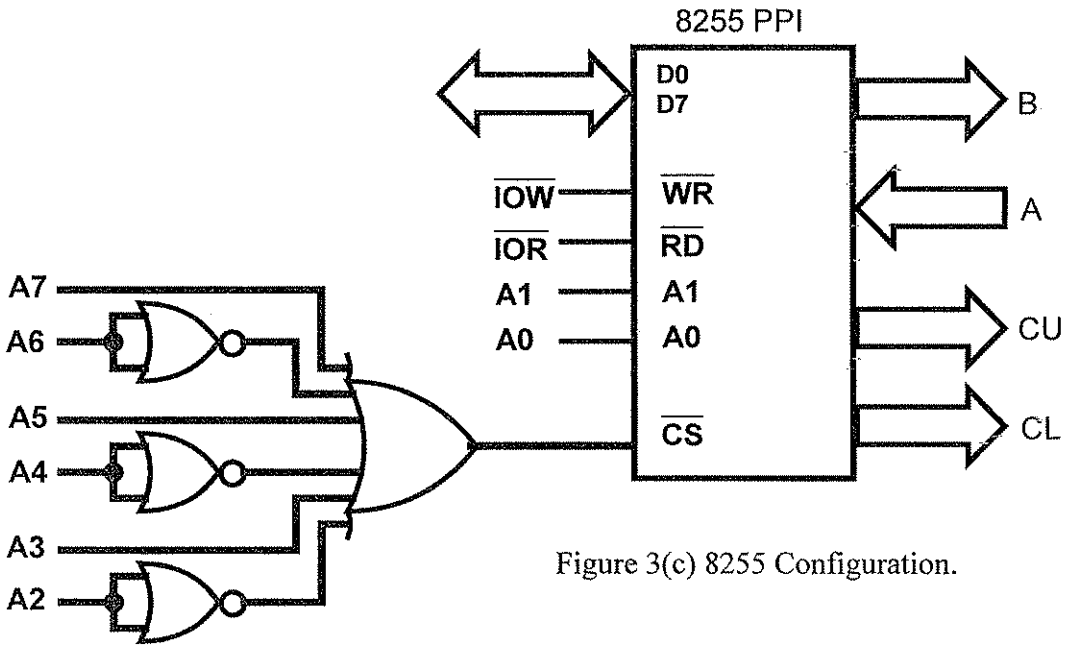

Figure 3(c) 8255 Configuration.

Question 4

(a) The 8259 PIC is configured as shown in Figure 4(a).

(i) Find the Initialization Control Words (ICWs) of the 8259 if it is used with an 8088/86 microprocessor, single, level triggering IRs, and IR1 is assigned "INT 18H". The 8259 is in master buffered mode with auto EOI and special fully nested.

(6 marks)

(ii) Write a program to initialize the 8259 using the port addresses in Figure 4(a). Also include comments for any instruction used.

(6 marks)

[Refer to Appendix E for 8259 PIC Control Words]

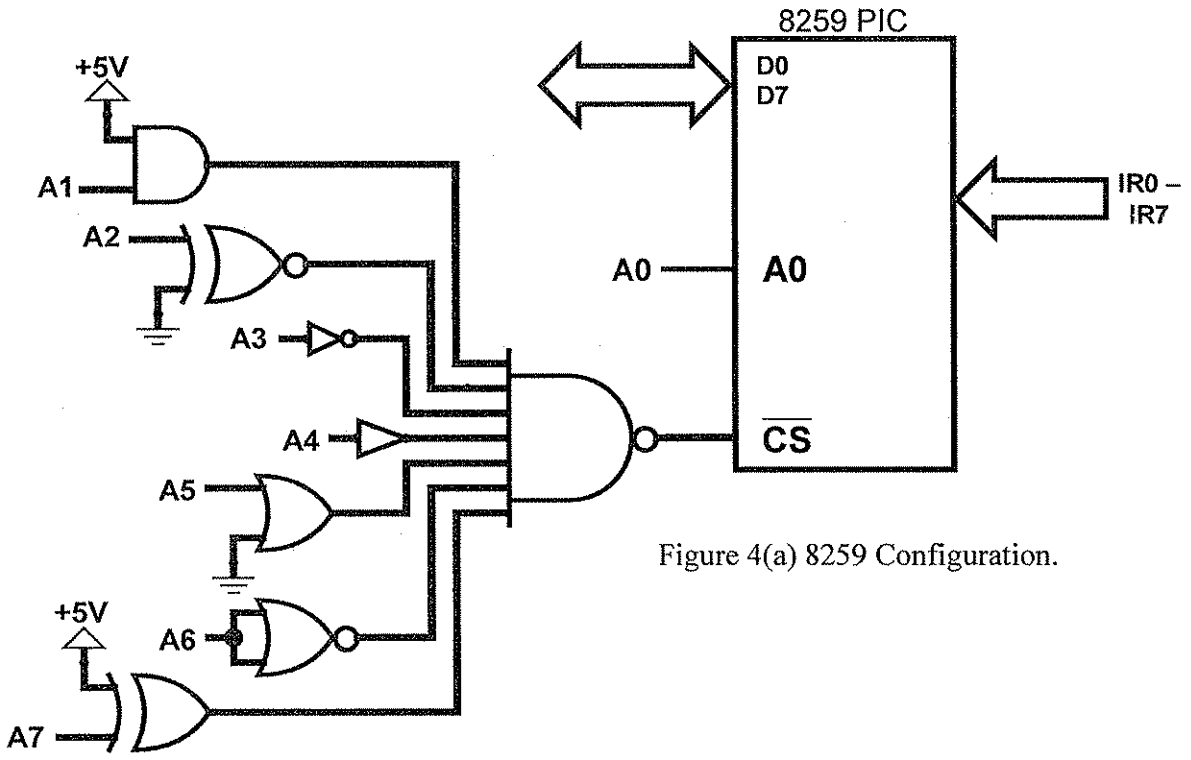

Figure 4(a) 8259 Configuration.

(b) Calculate the time delay taken for Program Q4(b) running on 8086 microprocessor at 5MHz. At a certain moment the state of an 8086 microprocessor based system is as follows: (All values are in Hexadecimal). Assume that DS register contains 0700H. Show all workings clearly for each instruction.

(13 marks)

[Refer to APPENDIX A for the cycle time]

	Memory															
	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
07500H	08	04	45	78	10	21	22	33	34	25	26	27	28	49	40	12
07600H	04	02	03	01	12	24	56	38	90	12	34	56	58	50	19	22

Table 4(b) Random Address Memory

Program		
	MOV	BX, [0602H]
	MOV	AX, 02H
LOOP2:	MOV	CX, BX
LOOP1:	NOP	
	LOOP	LOOP1
	DEC	AX
	JNZ	LOOP2
	HLT	

Program Q4(b) Coding.

Question 5

(a) The 8237 DMA is configured as shown in Figure 5(a). Determine the port addresses assigned to the four channels. Write a program using channel 3 memory address and count registers to transfer 8K starting from offset 4567H using the port address obtained. (5 marks)

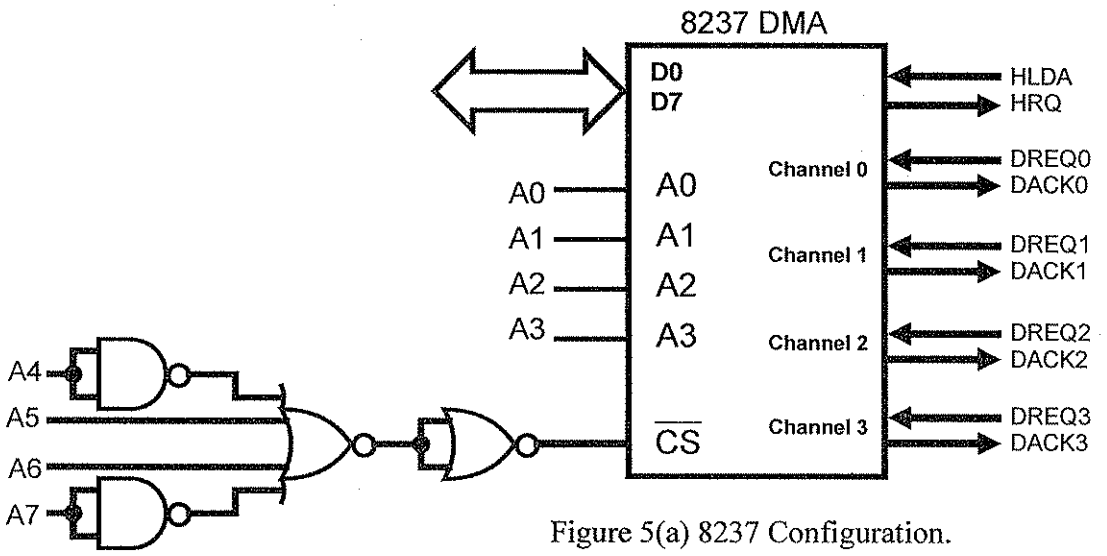

Figure 5(a) 8237 Configuration.

(b) A transmission system uses asynchronous serial data communication as shown in Figure 5(b) with LSB being transmitted first to transmit a passkey to the receiver.

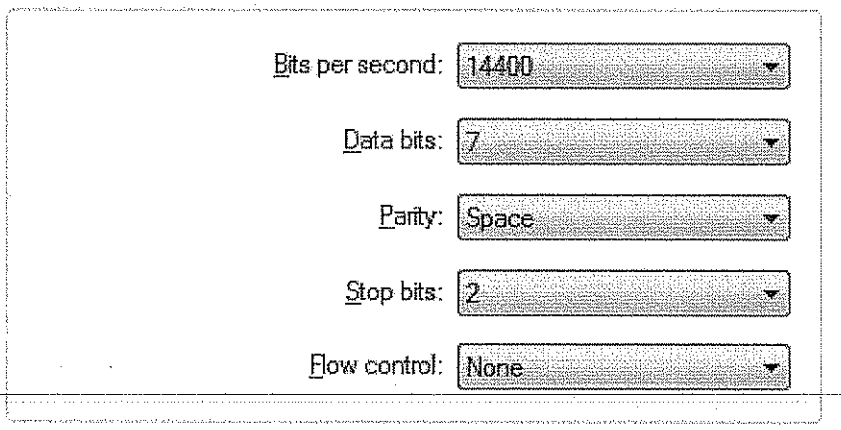

Figure 5(b) Serial communication settings.

Decode the following serial data received in continuous ASCII characters message:
Incoming data:
0101000101100000001011001011110110100110101101011010011001001100110100001100110000011001101010110011011111110011

(i) What is the passkey transmitted?

(11 marks)

(ii) Also, calculate the total time wasted due to overhead when transmitting the above message.

(3 marks)

[Refer to Appendix B for ASCII codes]

(c) Perform the following number system transformation. Show all workings clearly.

i) 2002.2002_8 to decimal equivalent.

(2 marks)

ii) $A6.B5_{16}$ to octal equivalent.

(2 marks)

iii) $[01010110_2 + 00010011_2]$ to BCD equivalent.

(2 marks)

Question 6

(a) Design an address decoding for the following memory mapping shown in Figure 6(a)(iii) using given decoder and any suitable logic gate(s) into the implementation. The designed circuit should be showing memory chips, microprocessor, buses and Read or Write connections. All memory chips are active low. Decoder (74LS138) information is as shown.

(15 marks)

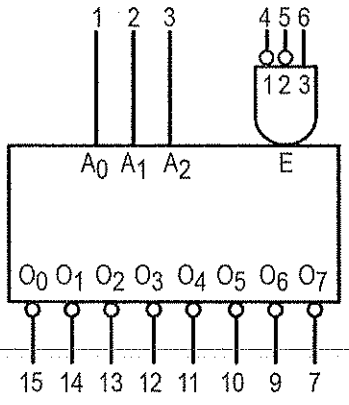

Figure 6(a)(i) Decoder: Logic symbol

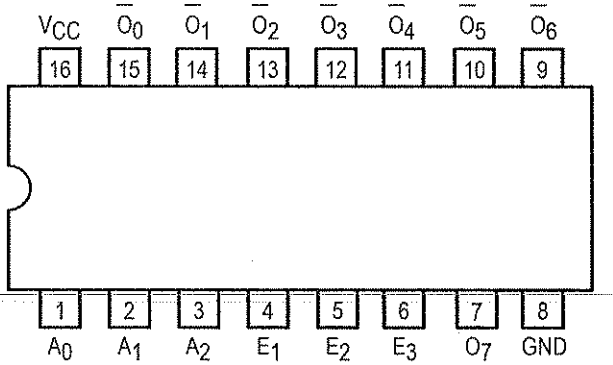

Figure 6(a)(ii) Decoder: Pin Configuration

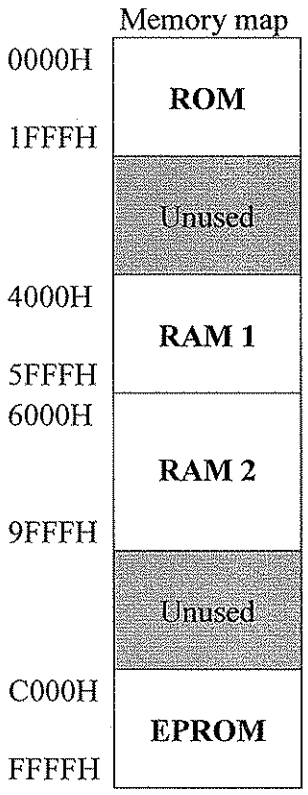

Figure 6(a)(iii) Memory map

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E_1}$	$\overline{E_2}$	E_3	A_0	A_1	A_2	$\overline{O_0}$	$\overline{O_1}$	$\overline{O_2}$	$\overline{O_3}$	$\overline{O_4}$	$\overline{O_5}$	$\overline{O_6}$	$\overline{O_7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Table 6(a) 74LS138 Decoder: Truth Table

(b) The 8254 PIT chip is configured as shown in Figure 6(b).

(i) Find the port address assigned to all the counters and the control register.

(2 marks)

(ii) CLK2 of counter 2 is 1.19318MHz and Gate2 is connected to high permanently. OUT2 of counter 2 is connected to IR0 (the highest-priority interrupt) of the 8259 interrupt controller to provide time-of-day interrupt (TOD) interrupt. Counter 2 uses a square wave to trigger the 8259. Write assembly instructions to divide this counter by 65,536. What is the OUT2 frequency?

(4 marks)

(iii) CLK0 of counter 0 is 1.19318MHz and Gate0 is connected to high permanently. Counter 0 generates a periodic pulse every 15.088μs to refresh DRAM memory of the computer. Write assembly instructions to generate this periodic pulse through OUT0.

(4 marks)

[Refer to Appendix D for 8253/8254 PIT Control Word]

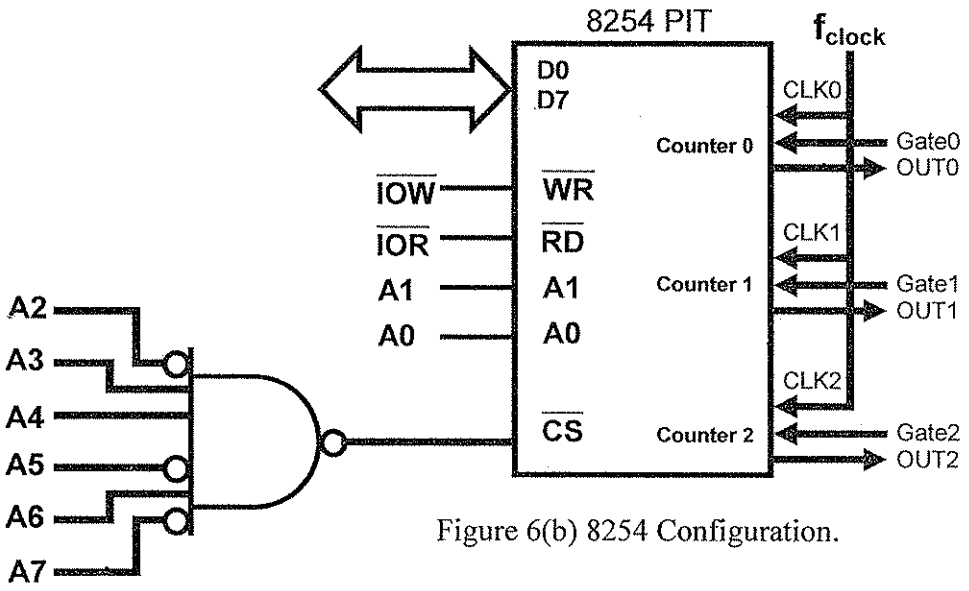

Figure 6(b) 8254 Configuration.

– THE END –