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INTERNATIONAL COLLEGE PENANG (507232-U)
LAUREATE INTERNATIONAL UNIVERSITIES

FINAL
Examination Paper

(COVER PAGE)

Session : APR 2014

Programme : DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING

Course : EEE 2101: INTRODUCTION TO DIGITAL ELECTRONICS

Date of Examination : 21 JULY 2014

Time : 5.00pm – 7.00pm Reading Time : Nil

Duration : 2 Hours

Special Instructions :

This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Students are not allowed to remove the question papers from the examination venue.

Materials permitted :
NON-PROGRAMMABLE SCIENTIFIC CALCULATOR

Materials provided :

Examiner(s) : Steven Khoo

Moderator : Dr. Khoo Bee Ee

This paper consists of 9 printed pages, including the cover page.

INTI INTERNATIONAL COLLEGE PENANG

DIPLOMA IN ELECTRICAL AND ELECTRONIC ENGINEERING PROGRAMME (DEE/I)

EEE2101: INTRODUCTION TO DIGITAL ELECTRONICS
FINAL EXAMINATION: APR2014 SESSION

Instructions: This paper consists of **SIX (6)** questions. Answer any **FOUR (4)** questions in the answer booklet provided. All questions carry equal marks.

Question 1

- (a) The logic circuit in Figure 1(a) below is used to control the drive spindle motor for a hard disk when the microcomputer is sending data to or receiving data from the hard disk. The circuit will turn on the motor when $DRIVE = 1$. Use the W, X and Y test points to assist in determining the input conditions necessary to turn on the motor.

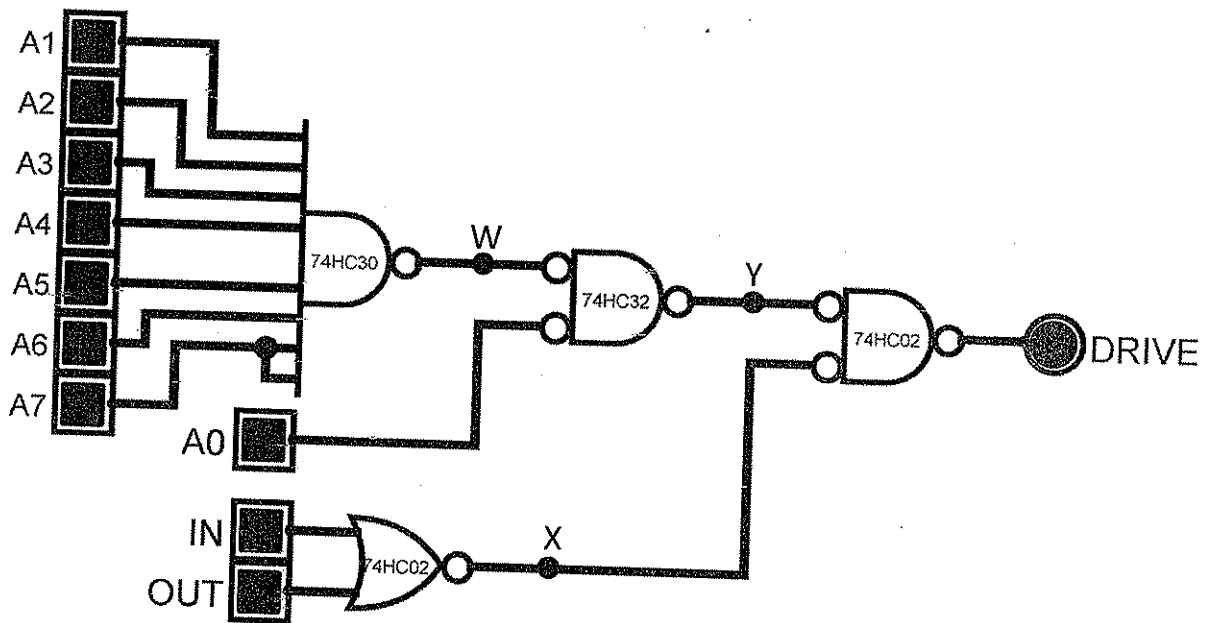


Figure 1(a)

(5 marks)

- (b) Table 1(b) shows the current ratings of TTL series logic gates. A 74ALS00 NAND gate output is driving three 74S gate inputs and one 7406 input. Determine if there is a loading problem.

(5 marks)

TTL Series	Outputs		Inputs	
	I_{OH}	I_{OL}	I_{IH}	I_{IL}
74	-0.4mA	16mA	40 μ A	-1.6mA
74S	-1.0mA	20mA	50 μ A	-2.0mA
74LS	-0.4mA	8mA	20 μ A	-0.4mA
74AS	-2.0mA	20mA	20 μ A	-0.5mA
74ALS	-0.4mA	8mA	20 μ A	-0.1mA
74F	-1.0mA	20mA	20 μ A	-0.6mA

Table 1(b)

The 74ALS00 NAND gate output needs to be used to drive some 74ALS inputs in addition to the load inputs. How many additional 74ALS inputs could the output drive without being overloaded?

(3 marks)

- (c) Perform the following number system transformation. Show all workings clearly.

i) 2002.2002_8 to decimal equivalent.

(3 marks)

ii) 138.135_{10} to hexadecimal equivalent.

(3 marks)

iii) $A6.B5_{16}$ to octal equivalent.

(3 marks)

iv) $[01010110_2 + 00010011_2]$ to BCD equivalent.

(3 marks)

Question 2

- (a) Prove that the Figure 2(a) with six (SIX) gates below can be simplified to a circuit using only 4 (FOUR) gates regardless of the types. Note that a NOT gate is also counted as one gate.

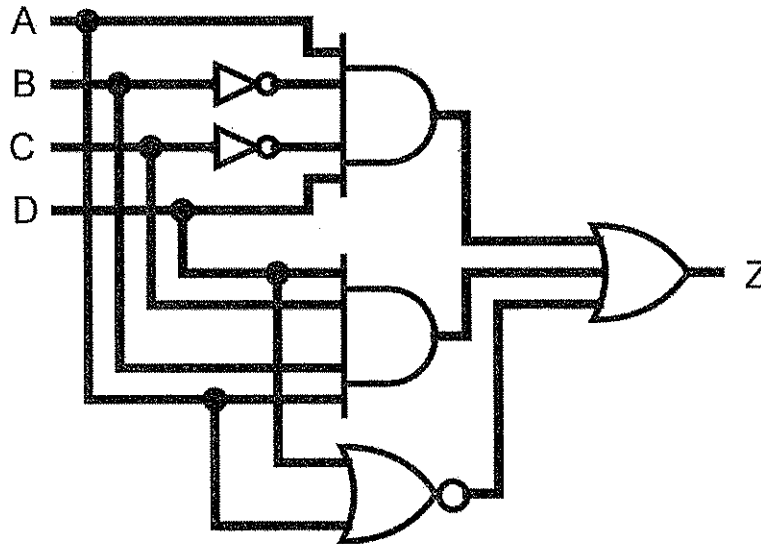


Figure 2(a)

(6 marks)

- (b) Determine the input condition(s) needed to produce $X = 1$ in Figure 2(b).

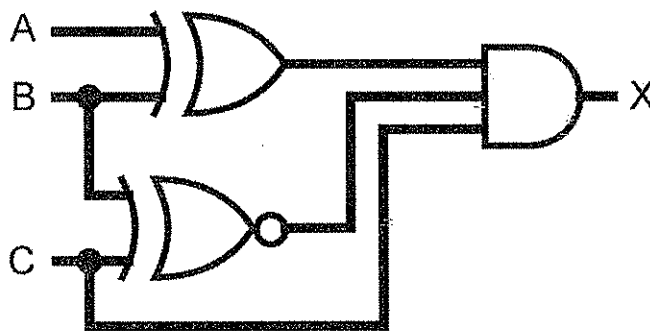


Figure 2(b)

(3 marks)

- (c) Figure 2(c) below shows a four-bit parallel counter which is designed so that it does not sequence through the entire 16 binary states. Analyse its operation by determining its counting sequence, and then draw the waveforms at each flip-flop output. Assume that all flip-flops are initially in the 0 state. Comment on the result obtained.

(16 marks)

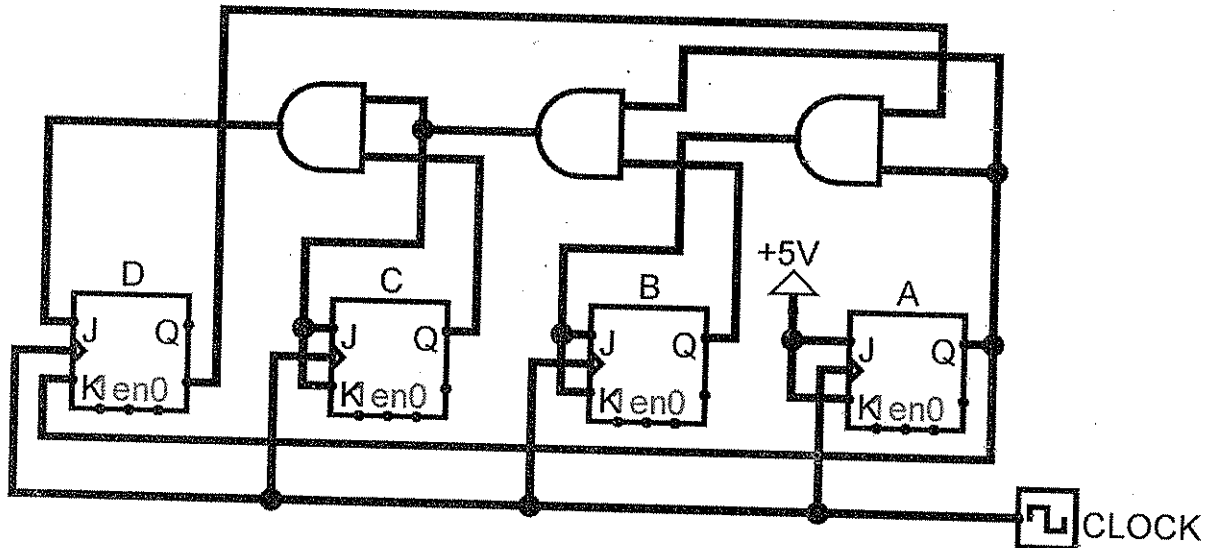


Figure 2(c)

Question 3

- (a) The logic circuit in Figure 3(a) generates an output, MEM that is used to activate the memory ICs in a particular microcomputer. Active-LOW is used to activate the memory ICs of a particular microcomputer. Use the V, W, X and Y test points to assist in determining the input conditions necessary to activate MEM.

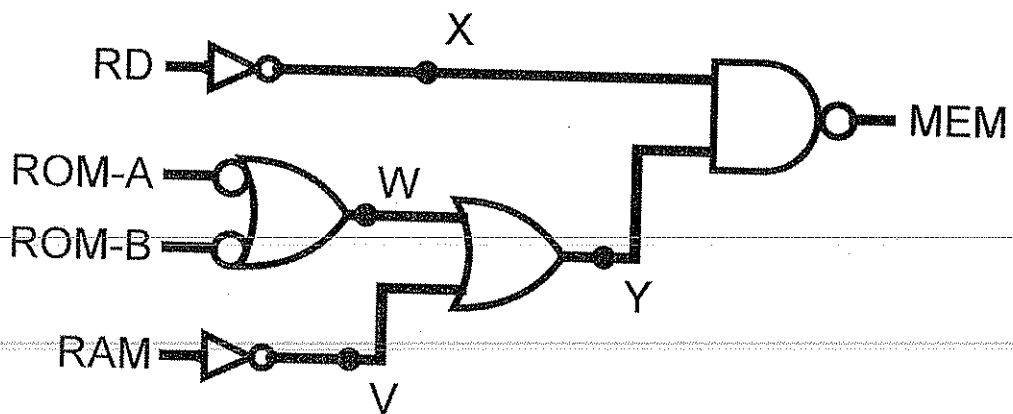


Figure 3(a)

(5 marks)

(b) Use Karnaugh map method to obtain the minimum

i) SOP expression for the function, $F(R, S, T, U) = \prod(2, 3, 6, 7, 9, 10, 12, 13, 14)$.
(4 marks)

ii) POS expression for the function, $F(W, X, Y, Z) = \sum(0, 2, 4, 6, 8, 10, 13, 15)$.
(4 marks)

iii) SOP expression for the function, $F(A, B, C, D) = \sum m(0, 4, 5, 8, 10, 15) + d(2, 7, 9, 13)$.
(4 marks)

(c) What is the 2's complement number of -3.625_{10} in signed numbering system? Determine the result of $2.25_{10} + (-4.75_{10})$ using 2's complement method. Prove that the final result is equal to -2.5_{10} in binary equivalents. Show the calculation working clearly.
(8 marks)

Question 4

(a) Design a synchronous 3-bit up/down counter using positive edge-triggered D flip-flop for MSB, JK flip-flop for second bit and T flip-flop for LSB. Assume all unused states as don't care. Input S will be used as the up/down control. The counter will count from $0 \Rightarrow 2 \Rightarrow 4 \Rightarrow 6 \Rightarrow 0$ when input, $S = 0$ and $6 \Rightarrow 4 \Rightarrow 2 \Rightarrow 0 \Rightarrow 6$ when input, $S = 1$. Provide proper labelling for the designed logic circuit. Show all workings clearly including all excitation tables used. Also, provide the state diagram with up/down conditions.
(15 marks)

(b) Figure 4(b) shows a computer controlling the speed of a motor. The 0 to 2mA analog current from the DAC is amplified to produce motor speeds from 0 to 1000 rpm (revolutions per minute). How many bits should be used if the computer is to be able to produce a motor speed that is within 2 rpm of the desired speed?
(5 marks)

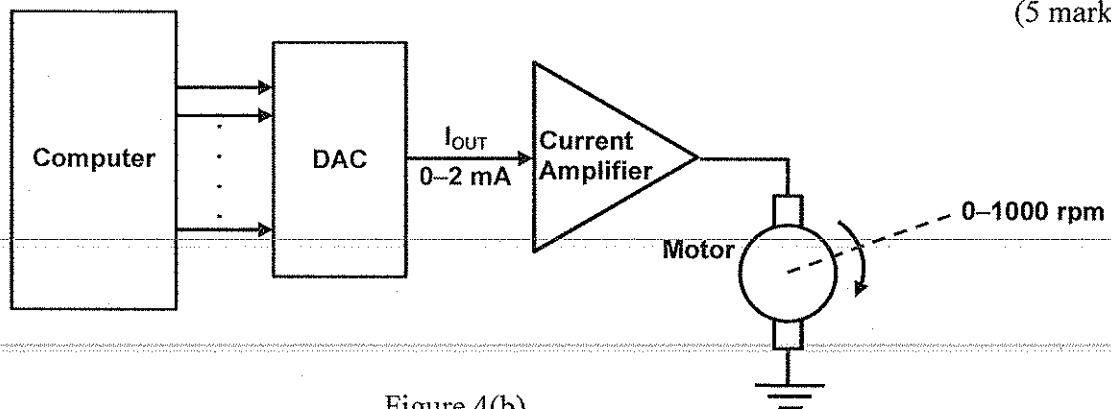


Figure 4(b)

Using the number of bits obtained, how close to 326 rpm can the motor speed be adjusted?
(5 marks)

Question 5

- (a) Figure 5(a) represents a relative-magnitude detector that takes two 2-bit binary numbers X_1X_0 and Y_1Y_0 and determine whether they are equal and, if not, which one is larger. There are three outputs, defined as follows:
1. $M = 1$ only if the two input numbers are equal
 2. $N = 1$ only if X_1X_0 is greater than Y_1Y_0
 3. $P = 1$ only if Y_1Y_0 is greater than X_1X_0
- Design the logic circuitry for this detector with minimum gates consideration. The logic circuit will have 4 inputs and three outputs.

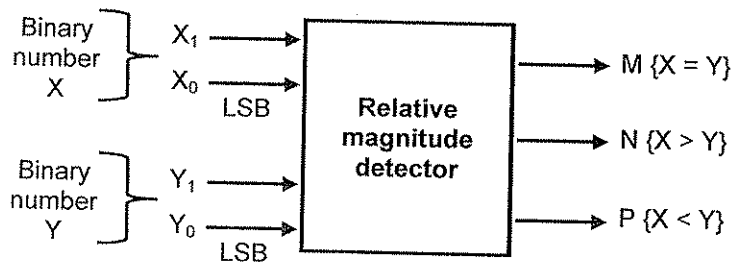


Figure 5(a)

(10 marks)

- (b) Figure 5(b) shows a simple DAC using an op-amp summing amplifier with binary-weighted resistors.

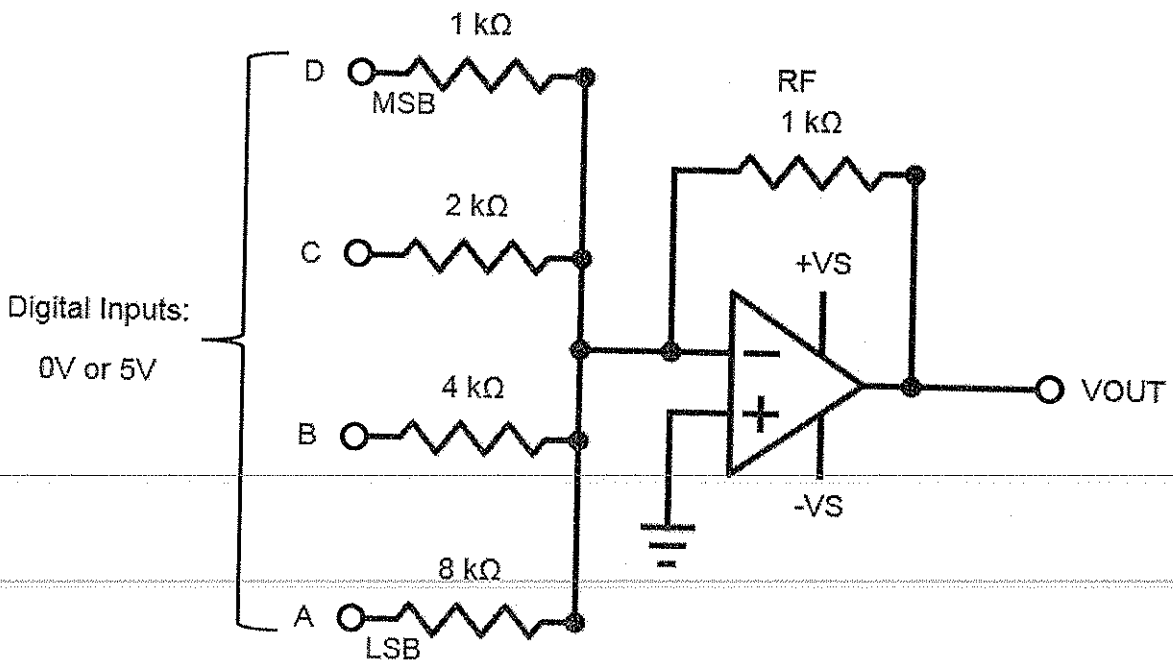


Figure 5(b)

- i) Determine the weight of each input bit of Figure 5(b). (4 marks)
- ii) Change R_F to 250Ω and determine the full-scale output. (3 marks)
- (c) Table 5(c) show a typical TTL series characteristics. Determine the noise margins when a 74LS device is driving a 74ALS input and when a 74ALS device is driving a 74LS input. (4 marks)

What will be the overall noise margin of a logic circuit that uses 74LS and 74ALS circuits?

(2 marks)

A logic circuit has $V_{IL}(\max) = 450\text{mV}$. Which TTL series can be used?

(2 marks)

	74	74S	74LS	74AS	74ALS	74F
Performance ratings						
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Max. clock rate (MHz)	35	125	45	200	70	100
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters						
$V_{OH}(\min)$	2.4	2.7	2.7	2.5	2.5	2.5
$V_{OL}(\max)$	0.4	0.5	0.5	0.5	0.5	0.5
$V_{IH}(\min)$	2.0	2.0	2.0	2.0	2.0	2.0
$V_{IL}(\max)$	0.8	0.8	0.8	0.8	0.8	0.8

Table 5(c)

Question 6

- a) Implement $F(A,B,C) = \Sigma(0,3,4,5)$ using the following in the simplest form:
- i) SN7408N (2-input AND gate), SN74ALS32N (2-input OR gate) and SN74ALS04BN (NOT gate). (4 marks)
- ii) SN7402N (2-input NOR gate) only. (4 marks)
- iii) SN74157N (2-to-1 Multiplexer) with A as select line and other logic gate(s). (4 marks)

iv) SN74LS138N (3-to-8 Decoder) and other logic gate(s).

Inputs				Outputs							
E	A ₂	A ₁	A ₀	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇
0	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0

(4 marks)

b) Refer to Figure 6(b) where an analog-to-digital converter is monitoring the dc voltage of a 15V storage battery on an orbiting spaceship. The converter's output is a 4-bit binary number, RSTU, corresponding to the battery voltage in steps of 1V, with R as the MSB. The converter's binary outputs are fed to a logic circuit that is to produce a HIGH output as long as the binary value is between $1000_2 = 8_{10}$ and $1100_2 = 12_{10}$; that is, the battery voltage is maintained between 8V and 12V. Design this logic circuit using only SN7400N (2-input NAND gates). Also, provide a truth table. Show all working steps.

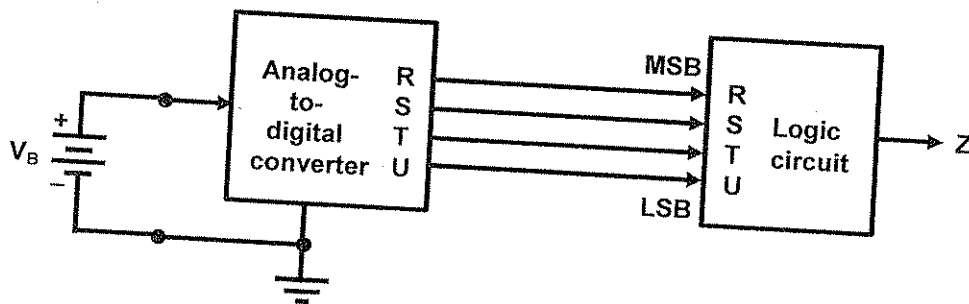


Figure 6(b)

(9 marks)

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